CISTER Quicknews

APRIL - JUNE ISSUE, 2018

CISTER organized and welcomed the premier event on Cyber-Physical Systems - CPS Week 2018 - from 10 to 13 April 2018 in Porto.

This year's edition features several events, including four top conferences, (1) ACM International Conference on Hybrid Systems: Computation and Control (HSCC), (2) ACM/IEEE International Conference on Cyber-Physical Systems (ICCPS), (3) ACM/IEEE International Conference on Information Processing in Sensor Networks (IPSN), and (4) IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS), and nearly twenty workshops, tutorials, competitions and foruns from both industry and academia.

CPSWeek was a great success with over 600 registrations from nearly 40 countries (nearly 1 out of 3 from the USA), including 450 registrations for the main conferences, 350 registrations for the workshops and tutorials and over 100 registrations for the competitions. The event also involved industrial sponsorship and participation from around the world including Microsoft Research, Denso, Mathworks, Toyota, NVIDIA, and Bosch.

Altogether, the CPS Week program covered a multitude of complementary aspects of CPS driven by leading researchers in the field. It was also a tremendous networking opportunity and visibility to the national CPS ecosystem. A team of 40+ persons was involved in the event from CISTER that took place in the historic Stock Exchange Palace in Porto.

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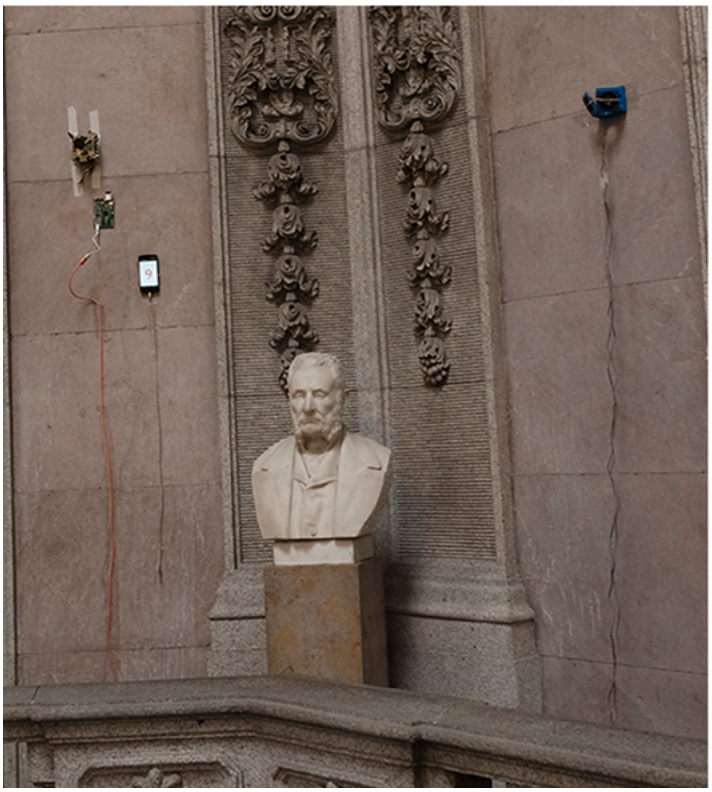
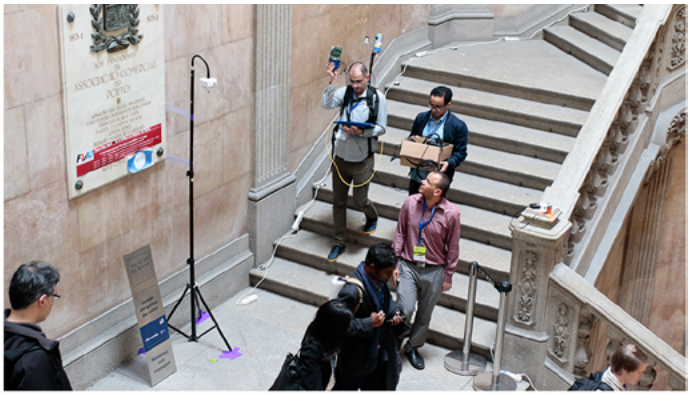
fundamental research activities

CPS Week 2018 included two major competitions in Porto.
The F1/10 Race and the Microsoft Indoor Localization took place during the Cyber-Physical Systems (CPS Week 2018) from 10 to 13 April 2018 in Porto.

F1/10 competition focus is to deliver challenging and significant design experiences to the students. The goal is to design, build and test an autonomous Formula One (F1) car in the 1/10 scale (capable of reaching speeds over 60 km/h) while exploring autonomous navigation concepts such as environment mapping, planning and control.
The car racing have been integrated into Cyber Physical Systems Week, the biggest event in the world in the cyber-physical systems field, and conference participants had the chance to watch the races in the main hall of Palácio da Bolsa.

Microsoft Indoor Localization competition focus is to evaluate and compare technologies from academia and industry in the same, unfamiliar space, by bringing teams to work in this area together in a more effective way.
Participants had to setup and calibrate their systems in the 8 hours of the first day of the competition. On the second day the systems where mounted on the evaluation backpack and a location log generated over a predetermined path in historic stairways of the building of Palácio da Bolsa.





CISTER Quicknews

APRIL- JUNE ISSUE, 2018

industry collaborations

ISO/IEC/JTC1 SC41 MEETING IN BERLIN

CISTER Researcher **Ramiro Robles** participated in the ISO/IEC/JTC1 SC41 meeting in Berlin, at the premises of the German standardization authority (DIN), where the SCOTT-ISO liaison between WG5 and the project SCOTT was accepted.

ISO/IEC JTC1/SC41/WG5 is the working group in charge of the Internet of Things technology and applications.
This activity is part of the standardization strategy of project SCOTT (Secure Connected Trustable Things).
Besides presenting and discussing the current state of the project with all project partners, the main goal of the meeting was to present the work on control of QEMU virtualization performed by CISTER's team.

REVIEW MEETING OF THE SAFECOP PROJECT

CISTER Researcher **Ricardo Severino** participated in the annual review meeting of the SafeCOP project in Brussels, where he presented an overview of the work carried out within the Safe and Secure Wireless Communications work-package, leaded by ISEP.

industry & projects

The work-package was quite successful and was approved by the reviewers. Ricardo also gave an overview of the progress in the Portuguese Vehicle Platooning Use Case being developed with GMVIS Skysoft.

PRESENTATION AND COMMUNICATION AWARD

SCOTT project won one of "Best Project Presentation and Communication Award" at the ECSEL JU Symposium 2018 in Brussels.

The ECSELJU Dissemination Award went to SCOTT and DEWI, another ECSEL JU in which CISTER participated as a partner, for an excellent job done to maximize the visibility of project results & future potential.

achievements in academia

INVITED TALK AT THE MPMM 2018

Michele Albano, as the leader of WP8 (Dissemination and Exploitation) of the MANTIS project, was invited to give a keynote speech at The Maintenance, Performance, Measurement and Management Conference 2018 (MPMM 2018), 21-23 June 2018, Coimbra, Portugal.
The title of the presentation was "Framework for Proactive Maintenance in the Real World" and provided a high-level overview of the work done in the project. The presentation comprised three different research directions: how MANTIS targets the problem of building a platform for the Proactive Maintenance of industrial machinery; how the involved technologies (CPS, cloud computing, machine learning and advanced HMI) are orchestrated together; how 4 different project pilots implemented the approach in a production environment.

CISTER Quicknews

APRIL - JUNE ISSUE, 2018

achievements in academia

CISTER RESEARCHERS SUCCESSFULLY DEFENDED THEIR PHD THESIS

Dynamic Contracts for Verification and Enforcement of Real-Time Systems Properties”

“Aerial Multi-Hop Sensor Networks”

“Dynamic Hierarchical Bandwidth Reservations for Switched Ethernet”

“Real-Time Software Transactional Memory”

CISTER Quicknews

APRIL - JUNE ISSUE, 2018

On the 5th of April of 2018, CISTER researcher **André Pedro** defended with success his PhD Thesis entitled **"Dynamic contracts for verification and enforcement of real-time systems properties"**. The evaluation committee included, among others, Professor Alan Burns from the University of York, United Kingdom, and Professor Simão Melo de Sousa, from University of Beira Interior, Portugal. The thesis defense took place in University of Minho.

André's PhD Thesis addressed the topic of Runtime verification, an emerging discipline that investigates methods and tools to enable the verification of program properties during the execution of the application, and its application to real-time embedded systems development, whose frameworks are still lacking support for the verification of properties using explicit time where counting time (i.e., durations) and that are fundamental for the development process. Based on a restricted fragment of Metric temporal logic with durations, the thesis presents novel synthesis mechanisms 1) for target systems as runtime monitors and 2) for SMT solvers as a way to get, respectively, a verdict at runtime and a schedulability problem to be solved before execution. The later is able to solve partially the schedulability analysis for periodic resource models and fixed priority scheduler algorithms. A domain specific language is also proposed in order to describe such schedulability analysis problems in a more high-level way. Finally, we validate both approaches, the first using empirical scheduling scenarios, and the second using the use case of the lightweight autopilot system Px4/Ardupilot.

Luis Pinto successfully defended his PhD thesis titled **"Aerial Multi-Hop Sensor Networks"** at FEUP in Porto.he thesis built on the growing interest in using Unmanned Aerial Vehicles (UAVs) for online monitoring applications, particularly inexpensive multi-rotors.

The proposal encompassed several small UAVs working collaboratively to provide extended sensing reach to operators on a ground station (GS). While a sub-group of the UAVs carried out the sensing function, another group set up an aerial multi-hop backbone to convey the sensing stream to the GS. Based on an experimental evaluation and modeling of the wireless link between two UAVs, the work led to three main contributions namely the Distributed Variable Slot Protocol that relies on TDMA with adaptive slot-length for coordinating transmissions, the Dynamic Relay Placement to mitigate links asymmetries by adjusting the position of the nodes in the backbone and a group navigation technique that increases the sensing rate in large areas. Altogether, these techniques bring significant benefits in terms of throughput, delay and reliability.

Zahid Iqbal successfully defended his PhD thesis titled "**Dynamic Hierarchical Bandwidth Reservations for Switched Ethernet"** at FEUP in Porto.His work addressed the case of distributed Cyber-Physical Systems (CPS) with a complex networking infrastructure, such as found in vehicles, buildings and industries, and aimed at providing technical, analytical and design tools to support composability and timeliness in dynamic settings.

For this purpose, his thesis claimed that a multi-level Hierarchical Scheduling Framework (HSF) could provide a solution, when applied to the most common communication technology in data-intensive CPS, namely Ethernet. A HSF provides hierarchical bandwidth reservations that enforce temporal isolation between different data streams intra and inter applications.

To support his thesis, Zahid made use of the Flexible Time-Triggered Switched Ethernet (FTT-SE) protocol, which allows deploying any traffic scheduling policy efficiently, including a HSF, in a dynamic manner.

On one hand, he provided a new worst-case network delay analysis for sporadic reservations associated with asynchronous messages, called flat reservations, and assessed its efficiency through extensive simulation.

On the other hand, he implemented multi-level HSFs using both polling and sporadic servers, verifying the strong partitioning capabilities of this approach and providing a novel method to generate polling server interfaces that minimizes the servers bandwidth requirement.

António Barros has successfully defended his PhD thesis, supervised by Luís Miguel Pinho, at the Faculty of Engineering of the University of Porto, Portugal. His thesis, entitled **"Real-Time Software Transactional Memory"**, proposes the use of Software Transactional Memory (STM) as a synchronization mechanism on multi-core systems with timing requirements. Although STM can be particularly more efficient than traditional lock-based approaches (especially if spatial and temporal isolation of code execution is required), the abort-and-repeat paradigm in which STM relies has a negative impact on the predicability of the response time of jobs and on the system demand.

This work studies the use of scheduling and contention management techniques that ensure application predictability. The PhD juri committee had as main examiners Mario Aldea Rivas (Assistant Professor, Facultad de Ciencias de la Universidad de Cantabria), Audrey Queudet (Assistant Professor, Faculté des Sciences et des Techniques, Université de Nantes) and Paulo Pedreiras (Assistant Professor, Departamento de Eletrónica, Telecomunicações e Informática,

CISTER Quicknews

APRIL - JUNE ISSUE, 2018

fundamental research activities

PERIODIC SEMINARS SERIES BY CISTER PHD STUDENTS

PhD student **Ishfaq Hussain** presented a talk on **"A Multicore Processor Platform for Energy and throughput Aware Applications"** at CISTER/ISEP.
In this talk,he discussed techniques to leverage the energy overhead due to the suboptimal utilization of available resources in multicore architectures while maximazing the throughput.
Ishfaq Hussain joined CISTER last 9th of April. He holds a Bachelor's degree in Science in Electrical Engineering and a Master's degree in Electrical and Electronics from HITEC University Taxila Cantt. Pakistan.
He has also worked for University of Sargodha as a Lecturer and for Emwi-Tech as a visiting researcher He has also been a Lecturer at University of Sargodha and a visiting researcher at Emwi-Tech. His area of specialization is energy/performance optimization in reconfigurable MPSoC architectures.

José Fonseca presented a talk on **"Response Time Analysis of Sporadic DAG Tasks for Global FP Scheduling"** at CISTER/ISEP.
In this talk he considered the global fixedpriority scheduling of sporadic real-time tasks, each one modeled by a directed acyclic graph (DAG) of parallel subtasks and derived a response time analysis (RTA) based on the concept of problem window.
José Fonseca joined CISTER in February 2012, his research activities are mostly related to the specification and analysis of real-time embedded systems, with particular emphasis on parallel applications. His main research interests include real-time operating systems, parallel programming models, real-time scheduling theory and multi-/many-core platforms.
Currently he is finishing his PhD studies in Electrical and Computer Engineering.

CISTER Quicknews

APRIL - JUNE ISSUE, 2018

CISTER DISTINGUISHED SEMINAR SERIES

Reinder Bril, associate professor at the Technical University of Eindhoven, The Netherlands, gave a distinguished seminar entitled **"Independent yet Tight WCRT Analysis for Individual Priority Classes in Ethernet AVB"** at CISTER/FEUP. Starting from the current motivations to use Ethernet technology to provide real-time communication the talk then focused on Ethernet AVB, a standard that enables transporting high-volume data (e.g. from cameras and entertainment applications) with latency guarantees. The traditional busy-period analysis that ensures these latency guarantees relies on knowledge of all interfering data streams. However, this is not realistic in complex industrial systems due to the high number of streams and the diversity of their patterns. Thus, the talk then presented an independent real-time analysis based on so-called eligible intervals, which does not rely on any assumptions on interfering priority classes other than those enforced in the Ethernet AVB standard. The analysis is proven tight when no additional information on interference is known.

CISTER Quicknews

APRIL - JUNE ISSUE, 2018

Moris Behnam, associate professor at Mälardalen University, Västeras, Sweden, gave a distinguished seminar entitled **"Predictability and dependability in parallel architectures"** at CISTER/FEUP. In this talk, he addressed the growing requirements for high performance, predictability and dependability guarantees of current industrial software applications, from trains to autonomous utility vehicles, aviation, smart grid power management and other. While the state of the art COTS hardware systems provide high performance through parallelization, achieving dependability and predictability is still challenging. The talk focused on results and ongoing activates within the "DPAC Dependable Platforms for Autonomous systems and Control" project, which considers multicore and heterogeneous system (including GPU and FPGA) architectures.

The project investigates how heavy parallel applications such as machine learning and video feature detection algorithms use low-level resources and tries to optimize their scheduling and allocation. Moreover, the project also investigates how to provide different levels of isolation between different applications sharing the system resources.

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