CISTER Quicknews

JUNE 2016

Progress in Projects

INITIATIVES FOR COOPERATION //

THE SMART ANYTHING EVERYWHERE INITIATIVE AND THE ADVANCED COMPUTING AND CPS COLLABORATION WORKSHOP

The "Smart Anything Everywhere" (SAE) is a Horizon 2020 initiative centered around networks of digital competence centers for supporting SMEs and mid-caps across the economy in digital value creation. These centers, usually research technology organizations (RTOs) or technology transfer-oriented university institutes, cluster a wide spectrum of technical and application knowledge to support digital innovation.

SAE innovation hubs gives SMEs an opportunity to experiment with new digital technologies, try them out in their processes and work together with technology suppliers to adapt it to their specific needs. In June, CISTER researcher Vincent Nelis represented CISTER at the SAE workshop organized in Brussels. The workshop brought together high-level speakers from the European Commission, industries, competence centers, and key players in European digital technologies to share ideas on topics related to the reindustrialization of Europe and the key role to be played by SMEs.

Also in June, Vincent Nelis gave a pitch on the P-SOCRATES project, an FP7 project led by CISTER, at the "Advanced Computing and Cyber-Physical Systems Collaboration Workshop", organized along with the SAE event by HiPEAC. This collaboration workshop brought together the "Cyber-Physical Systems", "Advanced Computing" and the "Mixed Criticality Systems" project clusters financed by the European Commission under FP7 ICT Call 10 (2013), H2020 ICT Call 1 (2014) and Call 4 (2015).

The main objectives of the workshop were to identify synergies and possibilities for cooperation between projects/participants; provide a better overall understanding for both the Commission staff and the project partners, of what is happening in this area of research and innovation, with possibility for Project Officers and project partners to informally assess the global progress; and identify and exchange of best practices, especially in the areas of standardization, exploitation, platform and ecosystem building.

ECSEL ENABLE-S3 kick-off meeting held

CISTER researcher David Pereira participated in the kick-off meeting of the recently approved ECSEL project ENABLE-S3. This project addresses the development and deployment of highly automated and autonomous cyber-physical systems, enabled by new functional, safety and security verification and validation approaches. CISTER participates in several work packages where research and development activities are going to take place in order to build the verification bricks that aspire to substitute today's cost-intensive validation and verification efforts by virtual and semi-virtual testing and verification in order to pave the way for efficient development of highly automated and autonomous systems. The project covers relevant use-cases arising from six different industry sectors, and CISTER participates in three of them - automotive, aerospace, and farming. ENABLE-S3 partners include AVL, Renault, Airbus Group, IBM, Magnetti Marelli, among many others, with GMV Skysoft acting as the key national industry player.

Final review of CONCERTO project

The final review of the CONCERTO project took take place in Brussels in the end of June. CONCERTO addressed the important challenge of simplifying and accelerating the design and development phase of the next-generation of mission-critical applications. The project is especially relevant in the context of constantly increasing complexity of functionalities to be implemented and the platforms on which they are deployed. CONCERTO proposes an integrated framework build around a component-based design approach following a model-driven development policy. It addresses all aspects of the system development lifecycle from application modelling to code generation. It incorporates runtime monitoring and verification features together with dependability and schedulability analysis tools. Several domain specific features have also been integrated for the avionics, automotive, petroleum and medical domains.

CISTER has been one of the first class contributors, leading the run-time monitoring and verification task and co-leading the task addressing the analysis of multicore systems. CISTER also largely contributed to tasks addressing domain specific needs for space, avionics, telecom and automotive. In Brussels, CISTER presented its numerous contributions in front of the european commission, which notably includes tools for schedulability and response time analysis of multicore systems, an Eclipse plugin for the automatic configuration of avionics system in an ARINC-653 compliant manner, a tool for response time analysis of Integrated Modular Avionics (IMA) systems, a run-time monitoring and verification library for systems written in Ada, a completely instrumented version of the ORK+ micro-kernel integrated in the GNAT cross-compiler for Leon 2/3 and an Eclipse plugin for treatment and back-propagation to application model of data monitored after application deployment.

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Achievements in Academia

CISTER researchers achieve outstanding results in ECRTS conference

CISTER researchers managed to continue their success in high quality ground-breaking research, with 4 papers accepted in the field of Real-Time Computing Systems, out of the 24 papers selected for publication, at the 28th Euromicro Conference on Real-Time Systems (ECRTS).

The selected papers where on topics such as Memory Contention & Overhead, Task Synchronization & Suspension, Scheduling and Schedulability Analysis. One paper, on Cache-Persistence-Aware Response-Time Analysis for Fixed-Priority Preemptive Systems (co-authored by CISTER researchers Syed Aftab Rashid, Geoffrey Nelissen, Benny Akesson, and Eduardo Tovar), received the "Outstanding Paper" distinction and has also been nominated for the "Best Paper Award".

ECRTS is one of the most reputed events in the field of Real-Time and Embedded Computing Systems, being one of the highly selective venues in which CISTER regularly and actively participates. It pairs with the IEEE Real-Time Systems Symposium (RTSS), whose 2016 edition is going to be co-organized by CISTER in Porto.

CISTER researcher co-chairs ADA-Europe

The International Conference on Reliable Software Technologies (Ada-Europe) conference has successfully established as an international forum in software technologies for critical embedded systems, with participants from both industry and academia. The 21st International Conference on Reliable Software Technologies, took place in Pisa, Italy, from June 13 to June 17, 2016. The conference was co-chaired by Marko Bertogna (Professor at University of Modena, Italy) and Luís Miguel Pinho (CISTER/INESC-TEC, ISEP).

Various topics of interest were present, under the general umbrella of reliable software systems, with a rich program of both scientific peer-reviewed papers (published by Springer LNCS 9695), industrial presentations, and tools demonstrations. Special focus was given to the topic of safe and predictable parallel software technologies. This is an important challenge for the design of smart cyber-physical systems,and is a topic being tackled by CISTER within the P-SOCRATES European project. A special session was dedicated to the integration of safe parallelism within the Ada language, a collaboration work being done by researchers and industrialists in USA, Canada and Portugal.

The conference also featured keynote talks, from Alan Burns, Professor at the University of York, UK, on programing languages for future cyber physical systems; Guido Ghisio, responsible for Automated Driving Technologies at Magneti Marelli, Italy, on challenges for the automotive platform of the future; and Marc Duranton, senior member of CEA, France, on the HiPEAC (European Network on High Performance and Embedded Architecture and Compilation) vision.

TACLe Summer School 2016

In late June, CISTER researcher Vincent Nelis gave a course on "WCET-aware parallel programming" at a summer school organized in Yspertal, Austria, by the ICT COST Action "TACLe". The objective of these lectures was to introduce young researchers to the types of timing requirements that are typically encountered in real-world applications, briefly survey the methodologies available for timing analysis, and weigh up their pros and cons under different contexts.

TACLe Timing Analysis on Code-Level

The lectures were focused, in particular, on modern applications that are subject to strict timing constraints but are also extremely demanding in terms of computation-power and thus need to execute on powerful architectures in which workload can be parallelized. This combination of high-performance and real-time requirements comes as a new and exciting challenge for the research community. Practical examples were also shown with simple programs on the Kalray MPPA-256 development board, collecting runtime timed traces, and using analysis tools provided in the Kalray SDK to get WCET estimates.

Activities in the Center

Visit of collaborator from Mälardalen University

Matthias Becker, a PhD student from Mälardalen University, Sweden, is visiting CISTER. Matthias' research focuses on many-core real-time systems with particular interest in predictable execution frameworks for industrial systems. This led to a close collaboration with CISTER's researchers Vincent Nélis and Borislav Nicolic. During a first visit in 2015, mechanisms for predictable execution on a clustered many-core processor were developed and later will be published at ECRTS 2016. During his current visit, Matthias is working on a prototype implementation of the framework targeting the Kalray MPPA 256 many-core processor. Additionally, he is working on extending the framework, taking other sources of unpredictability on a many-core processor into account. As part of the CISTER seminar series Matthias also presented the final outcomes of the ongoing collaboration. He will mainly present the developed execution framework and discuss future research directions.

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