HAPPY NEW 2017

CISTER had an eventful 2016 calendar with many important milestones.
CISTER continued its momentum, organising a top conference – RTSS 2016 - maintaining its publication portfolio in leading conferences and journals with over 60 publications, and four new projects: ENABLE-S3, SAFECOP, KhronoSim and DSGRID.

CISTER Quicknews

JANUARY 2017

happy new 2017!

CISTER has over the last few years placed significant effort in setting up a strong research infrastructure. This was especially trying given the period of global contraction and the dearth of national funding opportunities.
The long delayed evaluation, that had taken considerable resources of CISTER in the past, also took place. Nonetheless, the efforts towards attracting research students and staff, and the strategic target of CiTech and partnerships with industries has now started yielding results. This has also required CISTER to adapt and reshape its internal structure.
Looking ahead at 2017, our aim is to expand on these gains.
With our focused initiatives, we anticipate a good growth in research student intake. We aim to increase our participation in cutting-edge research projects and industry collaborations, both national and abroad.
For this, we intend to tackle competitive calls from ECSEL, H2020, PT2020 Co-promotion as well as Direct contracts. Our core areas of embedded and real time systems continue to have a strong fit with EU strategic research areas.
As an example, from 2017 onwards, CISTER will be involved in the Productive 4.0 European research project; this is a lighthouse EU initiative in Industry 4.0, a domain that has attracted considerable attention.
And finally, the upcoming iteration of the evaluation process will allow us to positively project our achievements and future strategic goals.
Also internally CISTER has started taking some important steps towards this aim. The definition of a new set of internal regulations, the re-election of Prof. Eduardo Tovar as the director as well as the reinforcement of the Board of Directors with new members, and, importantly, for the first time the election of a President of the Scientific Council, Prof. Pedro Souto. These, and further envisioned structural developments, enable us to formulate and implement the CISTER vision going forward.

We look forward to a productive year and wish you the same.

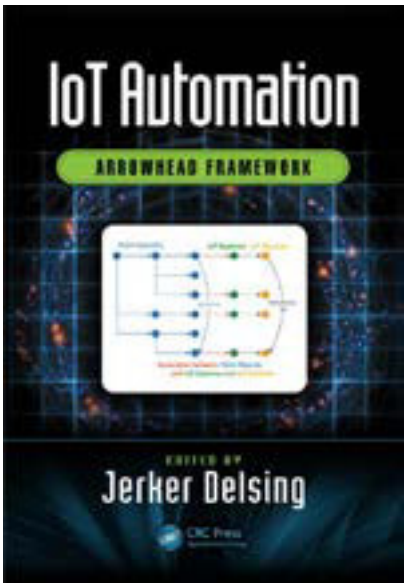
CISTER FOSTERS STRONGER RELATIONSHIP WITH FORMER RESEARCHERS

CISTER has a new initiative to increase interactions with former members of the unit to create new synergies from old partnerships. It's natural that previous members of a lab keep working in the same areas but, unfortunately, potential fruitful collaborations are often overlooked. This initiative looks to overcome this limitation by providing preferential bi-directional communication channels between existing and former researchers.
Areas that may benefit from this exchange include mobilizing new researchers, preparing project proposals, promoting exchange initiatives for students (PhD and others), provide strategic feedback and many others. Former CISTER members are now distributed around the world in Brazil, USA, South Korea, Singapore, India, Czech Republic, Sweden, France, Germany, Netherlands, United Kingdom and other countries.

achievements in academia

BOOK ON IOT AUTOMATION

CISTER researchers Luis Lino Ferreira and Michele Albano co-authored several chapters of the book "IoT Automation: Arrowhead Framework", which will be published in February, 2017 by CRC Press.



This book presents an in-depth description of the Arrowhead Framework and how it fosters interoperability between IoT devices at service level. This Framework is structured on the SOA technology and the concept of local cloud. The objective is to provide several automation capabilities such as: real time control, security, scalability, and engineering simplicity. The Arrowhead Framework supports the realization of collaborative automation; and it is the only IoT Framework that addresses global interoperability across multiple SOA technologies and therefore enabling the design, engineering, and operation of large automation systems for a wide range of applications utilizing IoT and CPS technologies.

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progress in projects

PARTICIPATION IN ECSEL PROJECT, PRODUCTIVE 4.0

CISTER will participate in the recently approved Productive 4.0 project, which will start in May this year. Productive 4.0 is an ECSEL lighthouse project, and one of the most important European initiatives in the ICT domain, connecting with the Industry 4.0 buzzword. Its main goal is to strengthen the international leadership of European industry.

The project will furnish companies with fundamental tools necessary to transform the potential of the upcoming digital revolution, known as Digital Industry, into business success. Productive 4.0 is focused on three main pillars: Digital Production (DP), Supply Chain Networks (SCN) and Product Lifecycle Management (PLM).

The idea focuses on digitised production applicable to all kinds of products. The results, such as IoT components modelling and simulation methods as well as toolchains for cross-lifecycle and cross-domain digitisation, are suitable means for linking all stages of a product lifecycle.

CISTER involvement in this project will focus on the evolution of its Quality of Service Framework for IoT applications, the reinforcement of a line of work coming from previous European projects such as Arrowhead and Mantis. This is in order to enhance its capabilities by being able to support more network technologies and integrate its capabilities with the Productive 4.0 toolchains.

ECSEL is an European Public Partnership in the areas of Nanoelectronics, Embedded Systems and Smart Systems joining together industry and Member States, with a R&D program encompassing a total proposed activity of close to €5 billion over seven years. The main objective of the work accomplished through ESCEL will be to accentuate the attractiveness of Europe for the high-tech industry and to contribute to the development of new technologies and applications that address tomorrow's main societal challenges.

RESULTS OF P-SOCRATES PROJECT PRESENTED IN STOCKHOLM

#HiPEAC17
January 23-25, 2017, Stockholm, Sweden

Last January, CISTER researcher Luis Miguel Pinho presented the results of the P-SOCRATES project in the 5th International workshop on the "Integration of mixed-criticality subsystems on multi-core and manycore processors". The workshop focused on solutions for the integration of mixed-criticality subsystems on multi-core processors, integrated in the HiPEAC 2017 conference.

The HiPEAC conference is the premier European forum for experts in computer architecture, programming models, compilers and operating systems for embedded and general-purpose systems. The conference attracted more than 500 participants from industry and academia from 37 countries.

The presentation both provided an overview of the successful outcomes of the P-SOCRATES project, as well as in particular focusing in the timing analysis methodology of the project, a technical work performed by the ISEP team in the project.

P-SOCRATES is an FP7 European project led by CISTER, a 3-year initiative that fosters the convergence of High-Performance Computing and Embedded Computing domains. The project developed methodologies and execution environments able to deliver high throughput, suitable for computationally-intensive applications, but also predictable throughput, so that guarantees can be provided on the responsiveness on the software functionality.

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activities in the centre

NEXT ENABLE-S3 GENERAL ASSEMBLY AT CISTER

The second General Assembly meeting of the ENABLE-S3 European project will be hosted by CISTER, and will take place on the 23rd and 24th of May 2017. The meeting will count with the presence of industrialists from key European players such as Airbus, AVL, Philips, Renault, Thales, among many others, as well as researchers from well-known European academic institutions.
The goal of ENABLE-S3 is to pave the way for accelerated application of highly automated and autonomous systems in the mobility domains of automotive, aerospace, rail and maritime as well as in the healthcare domain. Virtual testing, verification and coverage-oriented test selection methods will enable validation with reasonable efforts. The resulting validation framework will ensure European industrial competitiveness in the global race of automated systems with an expected market potential of 60B€ in 2025.
Project results will be used to propose standardized validation procedures for highly automated systems (ACPS).
During the General Assembly meeting, the latest developments and the next steps of the project will be discussed. The first prototype demonstrations of the various use-cases addressed by the project will also take place.

PEMAS VISITS CISTER

In January, representatives of the Portuguese Aerospace Industry Association - PEMAS visited CISTER.
During this fruitful meeting, CISTER researchers Eduardo Tovar and David Pereira had the chance to discuss with PEMAS representatives João Romana and Paulo Alexandre Chaves the current lines of action of the association and the role that CISTER can have on those actions, as the only academic partner of the association.
This was the first visit of PEMAS representatives to CISTER premises, and was a great opportunity for them to have a deeper understanding about the research being carried on in our unit, and of the CiTech initiative that is being leveraged by CISTER to enable the success of R&D produced by Portuguese actors working in Real-Time Embedded Computing and to boost their impact and role in the European innovation roadmap.

ARTEMIS/ECSEL BROKERAGE EVENT

CISTER researchers Luis Lino Ferreira and Eduardo Tovar participated in the 2017 Artemis Brokerage Event. The objective of this event is to help with the drafting of project proposals and finding the right consortium partners. Nearly 300 participants from prestigious European companies, Universities and Research Centres all over Europe attended this event.
During the brokerage, there was opportunity to discuss project ideas in the fields of Embedded & Cyber-Physical Systems, Internet of Things and Digital Platforms. The presentations on the Multi Annual Strategic Plan and Work Plan 2017 (MASP) where also illuminating. The main novelty being the definition of Safety and Security as an independent essential capability.

NEW RESEARCH STUDENT CALL

CISTER is happy to announce that it will soon open 4 PhD grants for candidate students willing to do research in Real-Time Embedded Computing.
We are looking for highly motivated candidates with a Master's degree in Electrical and Computer Engineering (ECE), Computer Science (CS), Software Engineering (SE), Applied Mathematics (AM) or related areas, and an excellent academic record. Candidates with solid industrial CV wishing to pursue a PhD degree are also encouraged to apply. Excellent spoken and written communication skills in English is considered essential.
The selected candidates will be given the chance to become part of an international and multi-cultural research team with a leading research track on multiple hot topics of RTES. CISTER's research environment is boosted by strong collaborations with various renowned academic institutions, such as the Carnegie Mellon University, the Technical University of Munich, the Max Planck Institute, the University of Pennsylvania, the University of York among many others, as well as with key international industrial players like Airbus, Volvo, Embraer, Honeywell, Critical Software, GMV or Bosch.
More info at *http://www.cister.isep.ipp.pt/jobs/*