CISTER Quicknews

JANUARY 2016

On December 10th, 2015, the third edition of the CISTER Industrial Workshop (CiWork 2015) took place in CISTER. On December 10th, 2015, the third edition of the CISTER Industrial Workshop (CiWork 2015) took place in CISTER. This workshop series brings together researchers and practitioners from industry and academia in a joint platform to debate recent developments and challenges (and their practical aspects in industry) in the emerging topic of embedded real time systems. The 2015 edition, like previous ones, was an opportunity for idea exchange and result sharing as well as approaches to challenges and technologies outlined in the recent national and international calls for projects. Industry attendees included EMBRAER, GALP Energia, Critical Software, EDISOFT, THALES, GMV, ISA, INOVA+ and IncreaseTime; while institutional representatives of IPP, INESC-TEC, ISEP and FEUP were also present. More information on the workshop and access to presentations is available at CiWork 2015. Previous editions are also available at CiWork 2013 and CiWork 2014.

SUCCESSFUL RESULTS IN ECSEL CALL

CISTER achieved excellent results in the 2015 ECSEL JU call with two proposals getting accepted, ENABLE-S3 and SAFECOP. ENABLE-S3 aspires to substitute today's cost-intensive validation and verification efforts by virtual and semi-virtual testing and verification, coverage-oriented test selection methods and standardization to pave the way for efficient development of highly automated and autonomous systems.

CISTER will participate in the requirement specification and implementation of three usecases (automotive, avionics, farming). The center will conduct studies to identify potential security and safety threats caused by unexpected non-functional, real-time behaviours, and develop supporting software toolboxes. It will also implement Runtime Verification components, and implement automated analysis tools for detecting the threats identified. Partners include major industrial partners such as AVL, Airbus, Renault, Toyota, Siemens and local partners GMV. SafeCOP addresses safety-related cooperating cyber-physical systems, characterised by use of wireless communication, multiple stakeholders, dynamic system definitions and unpredictable operating environments. CISTER will evaluate adequacy of COTS and standard wireless technologies, extend current wireless protocols for safe and secure cooperation and work on cooperative cruise control algorithms for platooning. It will also develop a multi-robot testbed for testing these algorithms for the vehicle platoon and bed transportation usecase. SafeCOP partners include Thalys, SINTEF, KTH, SICS and local partners GMV and Tekever.

We're on

CISTER - Research Center in
Real-Time & Embedded Computing Systems

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CISTER KEEPS INTERNATIONAL LEADERSHIP IN REAL-TIME AND EMBEDDED SYSTEMS

In the past 3 years, CISTER hosted and CISTER researchers were general chairs of several key international conferences such as SIES 2013, EWSN 2015 and ARCS 2015.

During that period, CISTER researchers were also general chairs of RTAS 2014 and program chairs of ECRTS 2013, RTAS 2013, ARCS 2014, WFCS 2014 and EWSN 2015, and were involved in over than 40 technical program committees of major conferences in the area of real-time and embedded computing systems, cyber-physical systems, reliable software, etc.

It is with deep satisfaction that we report that in 2016 this international scientific leadership will excel via the participation of CISTER researchers as program chairs of four major conferences in the area: ICCPS 2016, Ada-Europe 2016, RTCSA 2016 and RTNS 2016 and in a handful of workshops. This adds to the participation to the technical program committees of multiple other key scientific events in the area for 2016, including EWSN 2016, SIES 2016, WFCS 2016, ARCS 2015, ECRTS 2016, RTAS 2016, DATE 2016 or ETFA 2016. This rich and relevant participation in scientific service in 2016 involves most of the PhD researchers of CISTER.

SUCCESSFUL FINISH OF CARCODE PROJECT

The CarCoDe (Platform for Smart Car to Car Content Delivery) project developed a software platform for automotive domain which evokes the generation of the traffic service domain ecosystem. The tools for automotive, device and operating system independent software will allow third party developers to generate new innovative applications. Michele Albano represented CISTER at the final review meeting of the Portuguese CarCoDe project in November. In particular, the reviewers showed interest in the results of the simulations regarding efficient data dissemination in vehicular environment, and the use of the CarCoDe platform, developed by the Portuguese consortium, by the international partner of the project for their own demonstrators. The international CarCoDe had reached a satisfying completion earlier, and this last step of the Portuguese CarCoDe draws the ITEA-2 project to a positive close.

CISTER HOSTS LAST TACLE COST ACTION MEETING

On the 16th of November, CISTER Researchers Konstantinos Bletsas and Luís Miguel Pinho organized a TACLe ("Timing analysis at the code level") COST Action meeting in CISTER. COST Actions are designed to create networks of researchers in Europe around a particular topic. In this particular case, the meeting focused on the challenges in the timing analysis of many-cores especially with respect to parallel programs. Six 45-minutes talks were given during the meeting, each one followed by questions and answers. The speakers were Pr. Isabelle Puaut (University of Rennes/ INRIA, France), Ph.D. Vincent Nélis (CISTER/ISEP, Portugal), M.Sc. Michael Jacobs (Saarland University, Germany), M.SC. Leonidas Kosmidis (Barcelona Supercomputing Centre, Spain), Ph.D. Luca Santinelli (ONERA, France), and Ph.D. Sebastian Altmeyer (University of Luxembourg, Luxembourg)

MULTIPLE PHDS FROM CISTER'S RANKS

// Sven Goossens

Sven Goossens earned his PhD degree after defending his dissertation on the topic "A Reconfigurable Mixed-Time-Criticality SDRAM Controller" under the supervision of Benny Akesson. The work proposes two major contributions: (1) a new memory controller architecture, which supports run-time reconfiguration of its TDM arbiter, designed to target mixed-time-criticality systems and (2) a parameterization of the concept of memory patterns where composable read and write patterns can be generated with negligible performance loss. A unique feature of this memory controller is its conservative open-page policy that leaves rows open in the memory banks as long as possible to exploit locality and boost average-case performance, but closes them just in time to avoid reducing the worst-case performance. At the end of January, Sven starts his new career with Intrinsic-ID in Eindhoven. Best of luck to him with his new job!

// Ricardo Severino

Ricardo Severino has successfully defended his PhD Thesis at the Faculty of Engineering of University of Porto, Portugal. The Thesis, entitled "Improving Quality-of-Service for Large-Scale Wireless Sensor Networks", proposes a set of QoS improvement mechanisms for IEEE 802.15.4/ZigBee networks, which are validated and demonstrated over two real-world cyber-physical application scenarios, also engineered during his PhD. Ricardo scored 9 publications at top ranked venues, including one book chapter, 3 journal papers and 5 conference papers. The jury was composed of José Alfredo Ribeiro da Silva Matos (FEUP, representing the Rector), Leandro Buss Becker (UFSC, Brazil), Vlado Handziski (TU Berlin, Germany), Manuel Alberto Pereira Ricardo (FEUP), Paulo José Lopes Machado Portugal (FEUP), and his supervisor Eduardo Tovar (CISTER/ISEP).

// Claro Noda

MAPi DOCTORAL PROGRAMME IN COMPUTER SCIENCE

Claro Noda successfully defended his PhD degree in October, under the MAP-Tele PhD programme, a joint venture of the Universities of Minho, Aveiro and Porto. This programme is an unified effort to prepare highly qualified human resources in Telecommunications. The jury, composed by José Covas (U. Minho, representing the Rector), Rui Aguiar (U. Aveiro), Alexandre Santos(U. Minho), Jorge Sá Silva, (U. Coimbra), António Grilo (U. Lisboa) and also the co-supervisors Mário Alves (Politécnico do Porto) and Adriano Moreira, (U. Minho), granted Claro the highest possible classification of "Muito Bom". Claro's work focused on improving reliability and timeliness in low-power wireless networks (LPWN) under radio interference. During his PhD, Claro actively contributed to the MASQOTS national project (on reliable mobility support in LPWN) and to the CONET European NoE (in the Resource Management and Adaptation research cluster). Claro's work has been published at top-tier conferences including ACM IPSN (Best Paper Nominee), IEEE SECON and EWSN.

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CISTER RESEARCHER ORGANIZES LECTURES IN LULEA UNIVERSITY OF TECHNOLOGY

LULEÅ TEKNISKA UNIVERSITET

CISTER Researcher David Pereira, in collaboration with Prof. Per Lindgren of the Lulea University of Technology, organised and lectured an introductory course on deductive program verification, from the 22nd to the 27th of November. This is a PhD-level course for which the student who pass the class will get credits for their individual PhD plans. In this course, David Pereira was responsible for the theoretical classes, and in the near future, he will be involved in the evaluation of the practical works that will be assigned to the students.

AWARDS AND RECOGNITION AT CONFERENCES

RTNS 2015

CISTER received two out of the four "Outstanding Paper Awards" at the 23rd International Conference on Real-Time Networks and Systems (RTNS 2015), in November, in Lille, France. Alexander Esper, Geoffrey Nelissen, Vincent Nelis, and Eduardo Tovar received it for their paper titled "How Realistic is the Mixed-Criticality Real-Time System Model?" Another was received by Vincent Nelis for his paper titled "A Generic and Compositional Framework for Multicore Response Time Analysis".

CISTER SIGNS MOU WITH EMBRAER

EMBRAER

CISTER/ISEP and EMBRAER have signed a Memorandum of Understanding (MoU) in January to cement a long term collaboration. The Parties intent to build a cooperation relationship regarding research and development projects.

The purpose of this MOU is to establish the basis for a future collaborative relationship between the Parties regarding technology research and product development activities in subjects of common interest like digital communication in embedded real-time systems, multicore platforms in avionics applications and analytical and non-analytical methods for timing analysis in avionics networks.

The MoU will then be put into practice with the definition of a joint work plan for options such as direct contracts, joint projects and EU-FP initiatives.