CISTER Quicknews

NOVEMBER - DECEMBER ISSUE, 2018

NOMINATION FOR ASSOCIATE EDITOR FOR IEEE ACCESS JOURNAL

CISTER researcher **Kai Li** nominated as Associate Editor for IEEE Access Journal. As the Associate Editor, Kai Li is responsible for ensuring that the publication maintains the highest quality while adhering to the publication policies and procedures of the IEEE.

He will also help facilitate a rapid review process that takes less than two weeks, and coordinate the careful and critical review.

His research interests include vehicular communications and security, resource allocation optimization, Cyber-Physical Systems, Internet of Things, human sensing systems, sensor networks and UAV networks.

PARTICIPATION IN THE INTERNATIONAL FORUM EFECS 2018, IN LISBON

CISTER Researchers **Eduardo Tovar**, **Luis Lino Ferreira** and **Ricardo Severino**, attended EFECS 2018, that took place at the Lisbon Congress Centre - CCL .

EFECS 2018 is an international forum with a focus on 'Our Digital Future' along the Electronic Components and Systems value chain in Europe.

The organisers of this event, AENEAS, ARTEMIS-IA, EPoSS, ECSEL Joint Undertaking and the European Commission, in association with EUREKA, have joined forces to provide numerous opportunities to learn more about the latest developments, cooperation and funding possibilities in the ECS Community.

Several projects with CISTER participation were presented in the event, in the form of posters or in the form a small pitches. Additionally, CISTER members participated in several consortium building meetings, which will target the next Eureka and ECSEL calls.

5TH EDITION OF AED DAYS, IN OEIRAS

CISTER Researcher, **Cláudio Maia**, participated in the 5th edition of AED Days in Tagus Park, located in Oeiras, Lisbon.

AED Days is an event organized by the Portuguese Cluster of the Aeronautics, Space and Defence (ASD) Industries with the goal of gathering the main national and international ASD players to discuss the challenges and opportunities related to the ASD domain.

fundamental research activities

CISTER HAS GREAT PARTICIPATION IN RTSS 2018

CISTER Researcher **Geoffrey Nelissen** had three full papers presented at RTSS 2018. The three papers were the result of an ongoing collaboration with Scuola Sant' Anna in Pisa.

The presented papers discussed results in various but complementary topics such as resource sharing for self-suspending task, parallel DAG tasks scheduling in multicore platforms and memory feasibility analysis for parallel tasks executed on scratchpad based architectures.
"The SRP Resource Sharing Protocol for Self-Suspending Tasks" by **Geoffrey Nelissen**, and Alessandro Biondi at RTSS 18; "Memory Feasibility Analysis of Parallel Tasks Running on Scratchpad-Based Architectures" by Daniel Casini, Alessandro Biondi, **Geoffrey Nelissen**, and Giorgio Buttazzo, at RTSS 18; "Partitioned Fixed-Priority Scheduling of Parallel Tasks Without Preemptions" by Daniel Casini, Alessandro Biondi, G**eoffrey Nelissen**, and Giorgio Buttazzo, at RTSS 18.
CISTER researchers **Geoffrey Nelissen** and **Konstantinos Bletsas** gave two talks at the Workshop on Mixed Criticality Systems (WMC) held in conjunction with RTSS 2018.

Geoffrey gave an invited talk on the compliance of the mixed criticality systems model with industrial safety related standards.

Konstantinos presented a short paper as well as participated to a discussion panel on how the mixed criticality systems theory could be extended to integrate the notion of importance of a functionality for the system operation in addition of its criticality.
Both talks gave rise to very interesting discussions on the next possible evolutions of the mixed criticality systems model.

And also, CISTER Vice-Director **Luis Almeida** attended RTSS 2018 to participate in several meetings of the IEEE Technical Committee on Real-Time Systems. In these meetings, the venue for RTSS 2020 was chosen, which will be Houston, USA, and several executive decisions were taken concerning the steering of both RTSS and RTAS. Meanwhile, RTSS 2019 will take place in Singapore, going to Asia for the first time ever, while RTAS 2020 will take place within CPS Week 2020, as usual, this time in Sidney.

SCOTT GENERAL ASSEMBLY IN CORK, IRELAND

From the 16th until the 18th of October, 2018, CISTER Researcher **Ramiro Robles** participated in the SCOTT project consortium gathered in the city of Cork, Ireland for a face-to-face and General Assembly meetings.
This is the third General Assembly of the project and the second in 2018. This meeting was mainly used to keep track of the progress and to analyze the feedback from the reviewers after the meeting in Brussels in September 2018.
CISTER/ISEP plays a key role in the project as leader of the technology line of the reference architecture, chair of the technical board, and co-lead of the aeronautics use case.

SCOTT aims to build trust in IoT solutions for 5 different industrial domains: aeronautics, automotive, railway, building, and healthcare. SCOTT uses the concept of the Bubble to enhanced backwards compatibility with existing domain infrastructure, encapsulating these underlying technologies with a modern IoT interoperable and cross-domain cloud application environment with enhanced security, safety and trust.

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LAST GENERAL ASSEMBLY OF ENABLE-S3 PROJECT

CISTER researcher **David Pereira** has participated in the last General Assembly of the ECSEL project ENABLE-S3, that took place in Vienna, Austria, on the 10th and 11th of December.
The goal of this General Assembly was to start the preparation for the final review of the project, which will occur in May 2019, in Graz.
During the meeting, David interacted with use-case teams where CISTER is participating, defining the last actions that must be implemented for the final demonstrators.

achievements in academia

ANOTHER SUCCESSFUL PHD THESIS DEFENSE

Cláudio Maia has successfully defended his PhD thesis, supervised by **Luís Miguel Nogueira** and **Luís Miguel Pinho**, at the Faculty of Engineering of the University of Porto, located in Porto, Portugal.
His thesis, entitled **"Scheduling Parallel Real-Time Tasks in Multiprocessor Platforms"**, proposes to find efficient ways of dealing with the inherent parallel behaviour of multiprocessor platforms and ensuring application predictability by taking into account the shared resources in the platform.
The PhD juri committee had as main examiners Marko Bertogna (Associate Professor at the University of Modena and Reggio Emilia, Italy) and António Casimiro (Associate Professor at the University of Lisbon).

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fundamental research activities

DIRECTOR FROM CYSPRI LAB, IN AUSTRALIA,GAVE A TALK ON SECURITY IN INTERNET OF THINGS, AT CISTER

Sanjay K. Jha from Cybersecurity and Privacy Laboratory (Cyspri), Australia and the School of Computer Science and Engineering at the University of New South Wales (UNSW) gave a distinguished seminar titled "Care or Not Care: Security in Internet of Things (IoT)".

In the talk, he presented some results from his ongoing research projects on security of bodywork devices and Secure IoT configuration management. He also discussed about mechanisms to secure data provenance and location proof for wireless bodyworn sensing devices by exploiting symmetric spatio-temporal characteristics of the wireless link between two communicating parties.

Sanjay is Director of Cyspri at UNSW. He is the UNSW leader and IoT Security Theme leader of Cyber Security Cooperative Research Centre (CyberCRC) in Australia. He also heads the Network Systems and Security Group (NetSys) at the School of Computer Science and Engineering at the University of New South Wales. His research activities cover a wide range of topics in networking including Network and Systems Security, Wireless Sensor Networks, Adhoc/Community wireless networks, Resilience and Multicasting in IP Networks.

Sanjay has published over 200 articles in high quality journals and conferences and graduated 25 Phd students. He is the principal author of the book Engineering Internet QoS and a co-editor of the book Wireless Sensor Networks: A Systems Perspective.

Sanjay is an editor of the IEEE Trans. of Secure and Dependable Computing (TDSC) and served as an associate editor of the IEEE Transactions on Mobile Computing (TMC) and the ACM Computer Communication Review (CCR).had as main examiners Marko Bertogna (Associate Professor at the University of Modena and Reggio Emilia, Italy) and António Casimiro (Associate Professor at the University of Lisbon).

IN MEMORIAM

JOSÉ RUFINO (1958-2018)

José Rufino is a highly influential member of the Portuguese Embedded Real-Time Systems research community. His work set the grounds for many others researching on dependable real-time communication and safety-critical real-time software, and he produced a considerable body of work in collaboration with the European Space Agency.

He passed away this last summer, on the 29th of July, a shocking news that took us all by surprise. Jose Rufino, a professor at University of Lisbon, had frequent collaborations with CISTER and visited us for the last time in September of 2017 to participate in our 20th anniversary celebrations. Whoever came across Rufino will remember his acute critical eye in a somewhat shy and extremely kind character. Genuinely a good person.

So long Rufino!

CISTER - Research Centre in Real-Time & Embedded Computing Systems

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