CISTER
Research Center in
Real-Time & Embedded
Computing Systems

Annual Report

2014

isep Instituto Superior de Engenharia do Porto

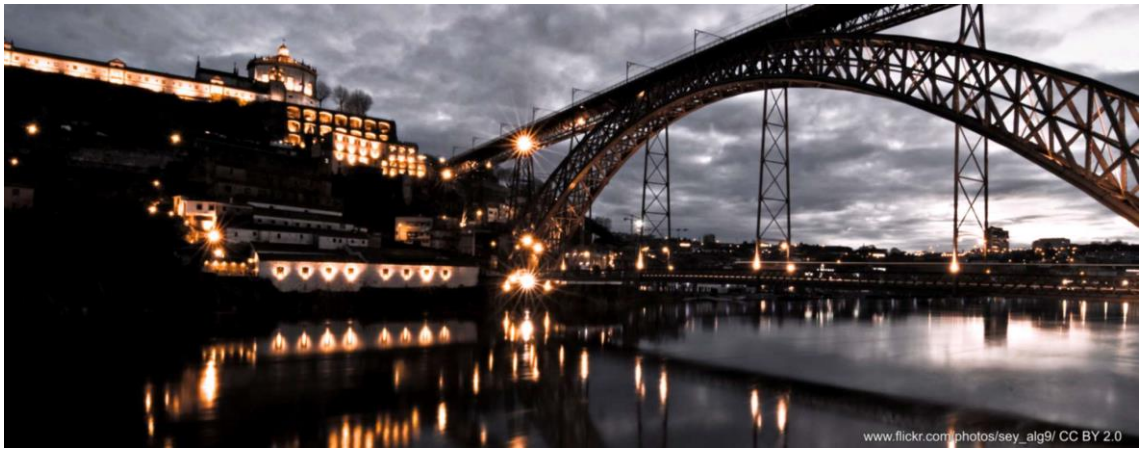
POLITÉCNICO DO PORTO

INESCTEC
TECNOLOGIA E CIÊNCIA

Contents

Executive Summary

www.cister.isep.ipp.pt



The Research Centre in Real-Time and Embedded Computing Systems (CISTER) is based upon a research group created in 1997 at the School of Engineering (ISEP) of the Polytechnic Institute of Porto (IPP). Since then it has grown to become the most prominent research unit of IPP and one of the leading international research centres in real-time and embedded computing systems. In both the 2003 and 2007 evaluation processes, the CISTER was granted the classification of 'Excellent' (the highest possible mark at that time) from an international panel of experts, being the only Portuguese unit in the areas of Electrical Engineering and Computer Science and Engineering to top-rank in both evaluations.

The strategy laid out by CISTER has been from the start towards top-quality research, able to compete with the best international groups in our research areas. The research activities is focused in the analysis, design and implementation of Real-Time and Embedded Computing Systems (RTES).

The goal of CISTER is to continue to be one the International leaders of research in real-time embedded systems, and naturally reinforce such privileged position. This objective is aligned with the growing strategic importance of RTES in Europe, and the role that needs to be played in the international research landscape of the area.

CISTER is hosted by ISEP, the main management institution. Since 2011, CISTER and ISEP have entered a strategic alliance with the INESC-TEC Associated Laboratory in which CISTER became an autonomous unit of INESC-TEC. It is our belief that this allows the continuation of the synergies in a challenging future environment.

Management Structure

The research unit is led by a Board of Directors, a Scientific Board and an External Advisory Board. The Board of Directors is led by the unit's Director and includes Vice Directors and an Adjunct Director. The main responsibilities of the Director are: to represent CISTER externally; to manage and co-ordinate the activities of the Unit; to co-ordinate the definition of the plan of activities and budget. The Scientific Board,

which includes all the members holding a PhD degree, has the following main responsibilities: to appoint the Director; to define the scientific research areas and working strategies; to carry out research; and to approve the plan of activities, budget and yearly report.

Board of Directors: Eduardo Tovar (Director), Luis Miguel Pinho (Vice-Director), Stefan M. Petters (Vice-Director), Filipe Pacheco (Adjunct-Director).

The activities of the unit are periodically reviewed by the External Advisory Board. Annually, interactions (including on-site visits) are organized to discuss activities, exploitation of results and future plans of the unit.

External Advisory Board: Tarek Abdelzaher, University of Illinois at Urbana-Champaign, USA; Sanjoy Baruah, University of North Carolina at Chapel Hill, USA; Alan Burns, The University of York, United Kingdom; Rodrigo Maia, Critical Software, Portugal; Daniel Mossé, University of Pittsburgh, USA; Michael Paulitsch, EADS, Germany; Sérgio Penna, Embraer, Brazil; Zlatko Petrov, Honeywell, Czech Republic; Raj Rajkumar, Carnegie-Mellon University, USA.

CISTER in Numbers

In 2014, CISTER has over 60 collaborators, covering more than 20 nationalities. Around one third of the researchers have PhD. This team has a strong and solid international reputation, built upon a robust track record of publications (70 publications in 2014), a continuous presence on program and organizing committees of international top conferences, as well as in pivotal industry-driven European projects.

CISTER is currently housed in an entirely new building exclusively devoted to its R&D activities. This single-home (2000 m2) is a strong asset to continue to compete among the best in the world in the area of RTES.

In 2014 the unit had around 1100K EUR of competitive funding. We had 8 international and industrial driven projects, and 9 fundamental research projects (FCT supported) running. We also got approved a set of new projects, accounting for a budget of 253K EUR in 2014, with a total budget of 750K EUR.

Focus and Research Lines

www.cister.isep.ipp.pt/research

CISTER focuses its activity in the analysis, design and implementation of Real-Time and Embedded Computing Systems (RTES). In these systems, correctness depends not only on the logical result of computation, but also on the time at which the results are produced. This implies that, unlike more traditional information and communication systems, where there is a separation between correctness and performance, in real-time systems correctness and performance are very tightly interrelated. Furthermore, considering their tight integration with the surrounding environment, RTES require a more holistic and integrated system perspective. Historically, RTES were an important, but narrow, niche of computing systems, consisting mainly of military systems, air traffic control and embedded systems for manufacturing and process control. Meanwhile, both the emergence of large-scale distributed systems and the pervasiveness of embedded devices, enabled by advances in technology, has broaden real-time concerns into a mainstream enterprise, with clients in a wide variety of industries and academic disciplines. This trend has established RTES technology as a priority for commercial strategy and academic research for the foreseeable future and also for a wider number of applications.

RTES technologies are deployed in almost all relevant market sectors across Europe. Consequently, they have a major impact on the way these sectors work and collaborate, how they will develop, how they are perceived by both professionals and the public, and how successful their products will be on the world market. RTES is one of the strategic research and innovation areas in Europe, with impact in very important sectors such as industrial automation, automotive, aerospace, consumer electronics, communication systems and medical systems. For many of these sectors, Europe is a world-wide reference, contrary to general-purpose computing systems, traditionally dominated by non-European organizations.

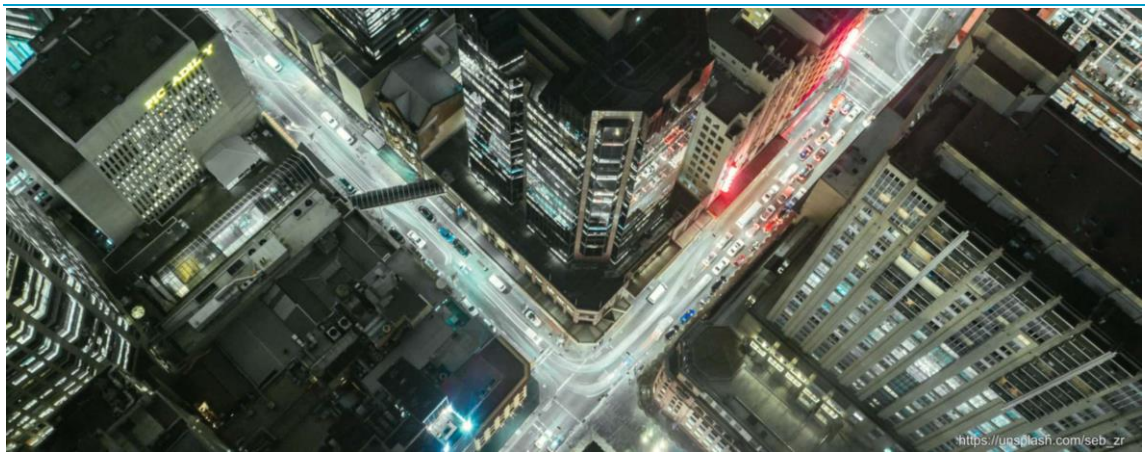
Wireless Sensor Networks (WSN)

Wireless Sensor Networks (WSNs) are triggering a new era in Information and Communication Technologies. These networks of tiny embedded computing systems are enabling a new set of large-scale monitoring and control applications such as pervasive Internet, homeland security, critical physical infrastructures monitoring, precision agriculture, environmental monitoring or intelligent transportation systems. CISTER has been assuming international leadership in the WSNs scientific area, namely on supporting Quality-of-Service (QoS), particularly focusing on timeliness and real-time, reliability and energy-efficiency aspects. We are addressing the use of both standard and COTS technology and cutting-edge solutions designed from scratch. CISTER pursues excellence-level collaborative R&D sustained by analytical, simulation and experimental models. We have recently designed, implemented and deployed the largest WSN test-bed in Europe to date, with 300+ sensor nodes.

Multicore Systems

Multicores are spreading at an unprecedented rate. Today, a multicore processor is the default choice in virtually any kind of standard computing device and it is increasingly being adopted in embedded computer systems (such as cellular phones, in-vehicle electronics and medical instrumentation).

The use of multicores in embedded systems is complicated by the fact that many embedded computer systems have real-time requirements, that is, the time at which a program produces its result is as important as the result itself. The time at which a program computes its result depends on how computer resources (processor cores, memory, bus bandwidth, I/O devices, etc.) are shared among programs and therefore the scientific community has created a toolkit of algorithms for scheduling programs on a single processor so that the program executes at the right time. Unfortunately, scheduling programs at the right time on a multicore is currently not well understood; in particular, there is no such well-established toolkit for multiprocessors. Researchers at CISTER are currently developing scheduling algorithms and proof techniques which makes it possible to prove at design time that deadlines will be met at run-time, even if the exact time when programs request to execute is unknown.



Cyber-Physical Systems (CPSs)

Although the IT transformation in the 20th century appeared revolutionary, a bigger change is probably yet to come. The terms "Cooperating-Objects" or "Cyber-Physical Systems (CPS)" have come to describe the research and technological effort that will ultimately efficiently allow interlinking the real world physical objects and cyberspace. Actually, the integration of physical processes and computing is not new. Embedded systems have been in place since a long time to denote systems that combine physical processes with computing.

The revolution will come from extensively networking embedded computing devices, in a blend that involves sensing, actuation, computation, networking, pervasiveness and physical processes. Such extreme networking poses considerable technical challenges ranging from the (distributed) programming paradigms (languages still lacking temporal semantics, suitable concurrency models and hardware abstractions) to networking protocols with timeliness as a structuring concern, and including systems theory that combines "physical concerns" (control systems, signal processing, etc.) and "computational concerns" (complexity, schedulability, computability, etc.).

Adaptive Real-Time Systems

We are increasingly surrounded by computer controlled devices. Many of which are not perceived as "computers" and are called embedded systems: think of mobile phones, cars, or aircraft. Many of these systems have some sort of real-time requirements, be it responsiveness, quality of service or hard deadlines, where the miss of the latter leads to catastrophic consequences. Beyond the fact that we are more and more surrounded and dependent on such systems, there is another trend visible. Embedded systems are often networked and/or receive upgrades and extensions during the lifetime of an individual system. These may be, for example, applications downloaded to your mobile phone or an upgrade of your motor control in a garage. A third trend is an increase in mobile systems, requiring effective power management to extend the battery lifetime.

Within this research line we address the issues associated with systems requiring temporal isolation of system parts with different criticalities, as well as systems being robust and reliable in the context of additional restrictions like available energy, changing environment or a dynamic set of tasks executed on such a system.

Real-Time Software

The current use of software as the key enabler of any real-time embedded system is increasing the often contradictory demands for attributes such as flexibility, adaptation, isolation, reliability or availability. Software infrastructure (such as languages, operating systems, middleware) and models are, more and more, a fundamental topic for system development, being transversal to application areas and research domains.

In this context, this research line addresses issues associated with the software infrastructure required for developing RTES. Our approach is to integrate advanced mechanisms within programming languages, operating systems and middleware, allowing designers and programmers to manage the increasing complexity, and flexibility requirements, simultaneously reducing common errors, and allowing isolation and verification of systems.

Research Projects

www.cister.isep.ipp.pt/projects

International & Industrial Driven Projects

Arrowhead

Ahead of the future

JU grant nr. 332987 ARTEMIS/0001/2012
Funding: 67.6MEUR (CISTER Funding: 207KEUR)

4 years (Mar 2013 to Feb 2017)

Our society is facing both energy and competitiveness challenges. These challenges are tightly linked and require new dynamic interactions between energy producers and energy consumers, between machines, between systems, between people and systems, etc. Cooperative automation is the key for these dynamic interactions and is enabled by the technology developed around the Internet of Things and Service Oriented Architectures.

The objective of the Arrowhead project is to address the technical and applicative challenges associated to cooperative automation: provide a technical framework adapted in terms of functions and performances; propose solutions for integration with legacy systems; implement and evaluate the cooperative automation through real experimentations in applicative domains: electro-mobility, smart buildings, infrastructures and smart cities, industrial production, energy production and energy virtual market; point out the accessible innovations thanks to new services; lead the way to further standardization work.

The strategy adopted in the project has four major dimensions: an innovation strategy based on business and technology gap analysis paired with a market implementation strategy based on end users priorities and long term

technology strategies; application pilots where technology demonstrations in real working environments will be made; a technology framework enabling collaborative automation and closing innovation critical technology gaps; an innovation coordination methodology for complex innovation "orchestration"

Partners of the Arrowhead consortium include, among others:

CarCoDe

Platform for Smart Car to Car Content Delivery

ITEA2 Nº 11037, QREN Nº 30345
Funding: 399KEUR (CISTER Funding: 58KEUR)

2 years (Jul 2013 to Jun 2015)

CarCoDe will develop a software platform which enables traffic service ICT ecosystems and business opportunities to be evoked. The objective is to offer a merging layer between automotive industry, traffic service operators, and third party developers. CarCoDe is an ITEA2 labeled European project. Portuguese partners are funded in the scope of a national QREN project.

Partners of the CarCoDe consortium include, among others:

CONCERTO

Guaranteed Component Assembly with Round Trip Analysis for Energy Efficient High-integrity Multi-core Systems

JU grant nr. 333053 ARTEMIS/0003/2012
Funding: 9.56MEUR (CISTER Funding: 375KEUR)

3 years (May 2013 to Apr 2016)

Emerging embedded systems platforms harnessing new heterogeneous, multicore architectures to enable the next generation of powerful mission-critical applications are demanding across-the-board advances in all areas of design and development to fulfil their promise. The integration of component-based design with model-driven development creates a potent combination especially capable of mastering the complexity of these new systems. CONCERTO will deliver a reference multi-domain architectural framework for complex, highly concurrent, and multi-core systems, where non-functional properties (including real-time, dependability, and energy management) will be established for individual components, derived for

the overall system at design time, and preserved by construction and monitoring at run-time.

The CONCERTO framework that will be developed in the project will integrate: Correctness-by-construction for multicore systems with innovative model-to-code transformation techniques targeted at their special characteristics. A multi-view, hierarchical cross-domain design space sufficiently rich to enable a compositional approach to the next generation of complex, heterogeneous platform architectures. Support for iterative and incremental development of multicore systems through simulation and early model-based analysis, with fully automated back propagation of results to the user model. Hardware modelling facilities equipped to cope with the new generation of heterogeneous, multicore platforms. Advances in run-time monitoring of mission- and operation-critical non-functional properties such as energy consumption on partitioned and multicore processor architectures. The applicability of the CONCERTO solutions to multiple industrial domains (including aerospace, telecoms, automotive, petroleum and medical) will be ensured through the elaboration of representative industrial use cases. CONCERTO builds on the previous CHESS project results from the ARTEMIS programme, as well as the results of several other related projects.

Partners of the CONCERTO consortium include, among others:

DEWI

Dependable Embedded Wireless Infrastructure

JU grant nr. 621353 ARTEMIS/0004/2013
Funding: 39.6 MEUR (CISTER Funding: 390 KEUR)

3 years (Jan 2013 to Dec 2015)

The EU project "DEWI-Dependable Embedded Wireless Infrastructure" with 58 partners from 11 countries deals with the development of wireless sensor networks and applications. DEWI deals with more than 20 industry driven application cases for citizens and professional users. The worked out results shall in conclusion be introduced to the public in all of Europe by using clear practical demonstrations in the areas of aeronautics, automobile, railroad and building automation.

Furthermore DEWI provides essential contributions to interoperability, standardization and certification of wireless sensor networks and wireless communication.

HiPEAC 3

European Network of Excellence on High Performance and Embedded Architecture and Compilation

FP7-ICT-287759
Funding: 3.8 MEUR

3 years (Jan 2013 to Dec 2015)

As part of the research coordination program, HiPEAC3 includes a new instrument, called Thematic Sessions. A Thematic Session is a natural evolution of the clusters and task forces in HiPEAC2, but more reactive and self-organized. In HiPEAC3, any partner or member can propose a thematic session, on condition that it is related to the HiPEAC vision. A thematic session is comparable to an informal workshop. Proposers of a thematic session are encouraged to involve the FP7 projects and HiPEAC companies in the session they propose. In that sense a thematic session is very similar to the organization of a cluster meeting in HiPEAC2. Collaboration and networking between member institutions and across the different disciplines: computer architects, design tool builders, compiler builders, system designers, between researchers from academia and industry, between European and non-European institutions. This collaboration between best of breed must lead to more European excellence in the HiPEAC domain. Collaboration and networking is stimulated by various networking events, and the small collaboration incentives like collaboration grants, mini-sabbaticals, internships.

Valorisation of research results in the form of highly visible publications and commercialization of research results by existing companies or by newly created companies. The goal is to help companies to achieve world-leading positions in the computing systems and computing products, and to further increase Europe's worldwide visibility in the domain via the HiPEAC conference, the ACACES summer school, the HiPEAC journal, a newsletter, a website, seminars, technical reports, workshops, and awards.

EMC^2

Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments

JU grant nr. 621429 | ARTEMIS/0001/2013
Funding: 94.6MEUR (CISTER Funding: 307KEUR)

3 years (Apr 2014 to Mar 2017)

EMC2 – 'Embedded Multi-Core systems for Mixed Criticality applications in dynamic and changeable real-time environments' is an ATREMIS Joint Undertaking project in the Innovation Pilot Programme 'Computing platforms for embedded systems' (AIPP5).

Embedded systems are the key innovation driver to improve almost all mechatronic products with cheaper and even new functionalities. They support today's information society as inter-system communication enabler. A major industrial challenge arises from the need to face cost efficient integration of different applications with different levels of safety and security on a single computing platform in an open context. The objective of EMC2 is to establish Multi-Core technology in all relevant Embedded Systems domains. EMC2 is a project of 97 partners of embedded industry and research from 19 European countries and Israel with an effort of about 800 person years and a total budget of about 100 million Euro.

P-SOCRATES

Parallel SOftware framework for time-CRitical mAny-core sysTEmS

FP7-ICT-611016
Funding: 2.76MEUR (CISTER Funding: 544KEUR)

3 years (Oct 2013 to Sep 2016)

The recent technological advancements and market trends are causing an interesting phenomenon towards the convergence of High-Performance Computing (HPC) and Embedded Computing (EC) domains. On one side, new kinds of HPC applications are being required by markets needing huge amounts of information to be processed within a bounded amount of time. On the other side, EC systems are increasingly concerned with providing higher performance in real-time, challenging the performance capabilities of current architectures. The advent of next-generation many-core embedded platforms has the chance of intercepting this converging need for predictable high-performance, allowing HPC and EC applications to be executed on efficient and powerful heterogeneous architectures integrating general-purpose processors with many-core computing fabrics. To this end, it is of paramount importance to develop new techniques for exploiting the massively parallel computation capabilities of such platforms in a predictable way.

P-SOCRATES will tackle this important challenge by merging leading research groups from the HPC and EC communities. The time-criticality and parallelisation challenges common to both areas will be addressed by proposing an integrated framework for executing workload-intensive applications with real-time requirements on top of next-generation commercial-off-the-shelf (COTS) platforms based on many-core accelerated architectures. The project will investigate new HPC techniques that fulfil real-time requirements.

The main sources of indeterminism will be identified, proposing efficient mapping and scheduling algorithms, along with the associated timing and

schedulability analysis, to guarantee the real-time and performance requirements of the applications.

Partners of the P-SOCRATES consortium include, among others:

cost-effective certification and re-certification of mixed-criticality, component based, multi-core systems.

Fundamental Research Projects

AVIACC

Analysis and Verification of Concurrent Critical Programs

FCOMP-01-012244-FEDER-020486 PTDC/EIA-CCO/117590
Funding: 94KEUR (CISTER Funding: 24.1KEUR)

3 years (May 2012 to Apr 2015)

The goal of the project is to extract models from concurrent programs and building an automatic framework for checking (temporal) properties using verification technologies, both static and run-time

MASQOTS

Mobility mAnagement in wireless Sensor networks under QoS constraints using standard and Off-The-Shelf technologies

FCOMP-01-0124-FEDER-014922 PTDC/EEA-TEL/112220/2009
CISTER Funding: 94.8KEUR

42 months (Feb 2011 to Jul 2014)

MASQOTS aims at real-time and reliable communications in IEEE 802.15.4/ZigBee (15.4/ZigBee, for short) Wireless Sensor Networks (WSNs) supporting physical mobility. Physical mobility concerns mobile sensor/actuator nodes and node groups (e.g. body sensor networks (BSNs), robots), and also mobile sinks (e.g. gateways, user-interface equipment).

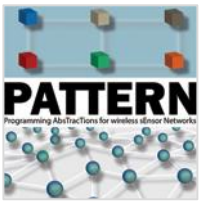
The main objective of this project is to design a real-time and reliable mobility management mechanism for IEEE 802.15.4/ZigBee-based WSNs.

We will build upon the most widespread WSN technologies – the 15.4 and ZigBee protocols and the TinyOS

operating system (OS) – for which the research team in this proposal is international leader. OnWorld predicts that in 2012, 88.3% of the WSN units will be standards-based. Freescale reports over 7 million 15.4/ZigBee units sold in 2008 and In-Stat forecasts 292 million units in 2012. TinyOS is the most used OS for WSNs.

MASQOTS will also address some fundamental (not yet solved) problems, such as the ones related to reliable Radio Link Quality Estimation (LQE), efficient and dynamic resource management, reliable and time-bounded handoff and re-association mechanisms and the provision of (simulation, analytical) models/tools for WSN analysis and dimensioning.

PATTERN



Programming AbsTracTions for wireless sEnsor Networks

FCOMP-01-0124-FEDER-028990 PTDC/EEI-SCR/2171/2012
CISTER Funding: 149KEUR

28 months (Jun 2013 to Sep 2015)

In this project, we aim to tackle two critical challenges for the future success of WSN: (i) provide a seamless model for the development of correct applications, whilst (ii) efficiently managing and isolating multiple independent applications.

Our WSN model and framework will seamlessly deploy multiple independent applications on a heterogeneous sensing infrastructure, coordinating computations, packet delivery and data aggregation to reduce overall resource usage. The programming framework is based on a macro programming approach and includes high-level programming abstractions. We plan to co-design the programming framework with adequate design patterns (a widely accepted software engineering approach).

We claim that such developments are crucial for future WSN and will be beneficial in many usage scenarios. This project particularly targets the use-case of modern smart buildings One important aspect of this application domain is that different users might develop them at different times, and it is not practical to merge them into a single application.

REGAIN

Real-time scheduling on general purpose graphics processor units

FCOMP-01-0124-FEDER-020447 PTDC/EIA-CCO/118080/2010
CISTER Funding: 139KEUR

40 months (Apr 2012 to Jul 2015)

Among all processors sold today, 98% are used in embedded computer systems; therefore, catering to this segment is of utmost importance. Moreover, there is a persistent trend in computing that techniques originally developed at the high-end (pipelining, cache-memories, instruction-level parallelism) later propagate to embedded computer systems. Graphics processors are the next technology to do this transition.

Therefore, this project will create a real-time scheduling theory for GPGPUs. This theory will offer (i) a model suited for describing real-time scheduling on GPGPUs, (ii) algorithms for run-time scheduling of tasks using GPGPUs and (iii) algorithms for proving, before run-time, that tasks using GPGPUs meet their deadlines. This project will also test the theory on commercially available GPGPUs.

RePoMuc

Real-time Power management on partitioned MultiCores

FCOMP-01-0124-FEDER-015050 PTDC/EIA-EIA/112599/2009
CISTER Funding: 106KEUR

3 years (Feb 2011 to Jan 2014)

The fundamental objective of the RePoMuC project to provide a methodology for real-time power-management in Multicores, considering: 1. the non-linear behaviour of dynamic frequency and voltage scaling (DVFS) on execution-time and energy, 2. pre-emption delays, and 3. memory bus contention Particular focus will be given to demonstrate with a real-world implementation the practicality and limitations of the proposed methodology. The approach I intend to take is to build on successful experience of the group in the areas of DVFS power management, real-time multiprocessor scheduling and temporal isolation. The issues of DVFS behaviour, pre-emption delays, and memory bus contention have a fundamental communality in the sense that they are all tightly coupled to the amount of memory traffic.

SMARTS

Slack Management in Hierarchical Real-Time Systems

FCOMP-01-0124-FEDER-020536 PTDC/EIA-CCO/121904/2010
CISTER Funding: 158KEUR

42 months (Apr 2012 to Sep 2015)

Most of modern computing systems are embedded with the physical environment. When such embedded systems are additionally subject to temporal constraints they are termed real-time systems.

There are a number of relevant trends in real-time systems: the complexity of such systems increases dramatically, often leading to integration of subsystems from various vendors; real-time and best effort applications may share the processor on a given device; the software on such systems may be subject to change leading to dynamic real-time systems.

A widely accepted design paradigm for such complex systems is component-based engineering in which 1) the system is first decomposed into simpler and smaller applications, 2) applications are independently designed and analysed, and 3) applications are composed together to generate the system. Depending on how the applications are grouped together for composition, the resulting system can be represented as a tree of applications; each parent-children pair denotes a composition where the child-applications were composed together to form the parent-application.

Within this project, we will: propose to investigate a comprehensive reclamation of all slack in a hierarchical system; investigate the impact of preemption, integrate pre-emption estimation techniques and provide a framework for alternative policies. Finally, we will explore how the developed techniques can be applied in a multicore setting.

For this we will build on the work of the ViPCore project (PTDC/EIA-CCO/111799/2009) also executed in CISTER, which in turn builds in among other things on [11, 27]. The multicore development will run in parallel to the other activities once the initial work on uniprocessors have been identified.

Smartskin

Densely Instrumented Physical Infrastructures

FCOMP-01-0124-FEDER-020312 PTDC/EEA-ELC/121753/2010
CISTER Funding: 141KEUR

3 years (Mar 2012 to Feb 2015)

Although the information technology transformation of the 20th century appeared revolutionary, a bigger change is on the horizon. The term Cyber-Physical Systems (CPS) has come to describe the research and technological effort that will ultimately allow the interlinking of the real-world physical objects and the cyberspace efficiently. The integration of physical processes and computing is not new.

Embedded systems have been in place for a long time and these systems often combine physical processes with computing. The revolution will come from massively networked embedded computing devices, which will allow instrumenting the physical world with pervasive networks of sensor-rich embedded computation.

In this project we intend to develop techniques and technologies that allow performing scalable and efficient data processing in large-scale dense cyber-physical systems. This is yet an unsolved problem. The major novelty of this proposal is effectively in the co-design of distributed algorithms for sensor data processing and underlying networked distributed computing systems with corresponding resource management schemes such that the utilization of resources is low.

VipCore

Virtual Processor-based Multicore Scheduling

FCOMP-01-0124-FEDER-015006 PTDC/EIA-CCO/111799/2009
CISTER Funding: 111KEUR

40 months (Feb 2011 to Jun 2014)

Scheduling on multicores is a much harder problem than those studied under single processor scheduling theories, largely because of the inherent non-parallelism in workload tasks. Although a multicore platform may execute different tasks from a workload at the same time, it is typically not allowed to execute the same task on more than one core simultaneously. This project plans to research multiprocessor frameworks and platforms to tackle these issues. One important concept is the notion of virtual processors, which allow to use a three-step scheduling strategy: partitioning of workload tasks and assigning virtual processors to each partition, scheduling of tasks on virtual processors within each cluster, and scheduling of virtual processors on the physical cores. Another important concept is the notion of pJobs, which allow tasks to be executed in parallel in the physical cores, increasing the potential parallelism of applications. The project will also research into architectures and platforms for supporting these concepts, and the underlying resource sharing paradigms.

V-SIS

Sistema de Validação de Sistemas Críticos

QREN - SI I&DT Nr. 38923
CISTER Funding: 53KEUR

18 months (Jan 2014 to Jul 2015)

The technological and scientific evolution is not linear. Like a river that forms during a storm the evolution droplets accumulate up until when they gather sufficient momentum to create a torrent or change the course of a river. This landscape of change is taking place these days in the development and validation of critical systems in the automotive and aeronautics sectors. The effects of this change also propagate to sectors like medical equipment and railway. The competence to validate highly optimized and high-value critical systems is essential for an economy like Portugal that has to compete with economies that build their strength in "brute force" with cheap labour. The V-SIS project proposes addressing this challenge with the creation of a critical systems validation competence centre, leveraging our capability to compete worldwide. The project seeks to take advantage from the landscape of change, the doubts and needs triggered by normative evolutions like the ISO26262 inception (automotive) and the upgrade to DO-178C (avionics). The V-SIS project proposes working two elemental vectors (1) functional safety and (2) critical systems validation. The work will be arranged in (i) processes innovation (RAMS techniques, model based V&V, multi-criticality systems, security fault injection) and (ii) validation laboratory development.

Highlights 2014

www.cister.isep.ipp.pt/news

January

Another ARTEMIS Project approved for 2014

DEWI (Dependable Embedded Wireless Infrastructure), another ARTEMIS project where CISTER participates was approved. This is another result of the effort developed by CISTER in the last open call for research projects in the strategic ARTEMIS initiative. DEWI is scheduled to start March 2014 and EMC2 (Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments) an Artemis Innovation Pilot Project (AIPP) in April 2014.

DEWI envisions to significantly foster Europe's leading position in embedded wireless systems and smart (mobile) environments such as vehicles, railway cars, airplanes and buildings. Each of these environments is reflected as a domain in the project, and CISTER's main work is in the Aeronautics domain (SP2), led by CISTER researchers. CISTER is also involved in management and architectural work in the Interoperability domain (SP6) that is responsible for finding commonalities between the several application domains.

DEWI is also a success case as it has the biggest industrial Portuguese participation in an Artemis project. Besides CISTER, the project involves Critical Software, Critical Materials and GMV.

HiRES Workshop at HiPEAC 2014

CISTER researcher Luis Miguel Pinho co-organized the 2nd Workshop on High-performance and Real-time Embedded Systems (HiRES 2014) held in conjunction with the 9th International Conference on High-Performance and Embedded Architectures and Compilers (HiPEAC 2014).

The workshop (which occurred on January 20, 2014, in Vienna, Austria) brought together researchers and engineers in the confluence of high-performance, embedded and real-time systems for a variety of application domains. As usual, the event was fruitful with discussions on the challenges and research directions that should be tackled by the community.

The program counted with one keynote from Thorbjörn Jemander, Vision Software Architect at Autoliv Electronics (Sweden), presenting a perspective on the challenges of HPC techniques when applied to automotive critical systems. Additionally there were two sessions of technical papers on topics such as many-cores, mixed-criticality and parallelization, and a session on presentations from European R&D projects on the area. The workshop was a success, doubling the number of participants from the previous edition, and almost doubling the number of submitted papers.

CISTER/INESC-TEC Seminar on Appliance's Energy Efficiency under Peak Power Constraints

Last January 21st, 2014 CISTER hosted another of its seminars, this time dedicated to energy efficiency. The seminar titled "Coordinated Scheduling of TCEDs under Peak Power Constraint" was given by Gopinath Karmakar from the Bhabha Atomic Research Centre, India, and addressed the problem of maintaining thermal comfort-bands associated with background loads under Peak energy consumption constraint.

Peak energy consumption has impact on upfront capital costs and hence on energy tariffs. Reducing the size of the peaks has been recognized as an important consideration in the design of efficient demand-response systems. A substantial fraction of the energy demand of buildings comes from the Thermostatically Controlled Electrical Devices (TCED) viz., air-conditioners (ACs), refrigerators and room-heaters, which do not need human interaction for their continuous operations.

So long as desirable temperature levels, referred to as thermal comfort-bands, are maintained by such background loads, users will not be concerned about when they perform their assigned functions. i.e., when they consume the energy required to function. Thermal Comfort Band Maintenance (TCBM), a new algorithm for scheduling such background loads under peak power constraint was presented as well as a discussion on how TCBM can adapt to changes in ambient parameters and provide the basis for efficient demand-response systems.

Gopinath Karmakar is a scientist from the Bhabha Atomic Research Centre, India, which has been involved in the design and development of embedded software for safety-related systems of the Indian nuclear plants for more than two decades. His current research interest is smart grid with a focus on smart home.

TACLe COST Action Meeting

CISTER researcher Konstantinos Bletsas attended the TACLe ("Timing analysis at the code level") COST Action meeting in Vienna, January 23-24, representing Portugal in the "Management Committee".

The two days meeting involved research presentations from participants and discussion in between. The meeting also included managerial sessions where

planning and decisions about the project where discussed and agreed; namely, the planning of TACLe summer school this year.

COST Actions are designed to create networks of researchers in Europe around a particular topic. In this particular case, it concerns code-level timing analysis and brings together researchers from key research organizations in Europe, like the Mälardalen University, Sweden, University of York, UK, or University of Saarbrücken, Germany.

Arrowhead General Assembly Meeting and first review results

CISTER researchers Luis Lino Ferreira and Christos Chrysoulas participated on the Artemis AIPP Arrowhead General assembly which has been held in Budapest, on January 14th-16th.

During the meeting the participants had the chance to present, discuss and apply the Arrowhead Documentation Framework and the Arrowhead Common Framework. The former is being developed on task 7.1 led by CISTER, and the later being developed in task 7.3 and WP8, with a strong participation by CISTER.

Also during the meeting, the participants had the possibility of analyzing the very positive results of the first project review meeting and that the commission accepted all deliverables submitted by the project consortium.

The Arrowhead project addresses cooperative automation and is enabled by the technology developed around the Internet of Things and Service Oriented Architectures. The project will provide a technical framework adapted to such systems. Implementation and evaluation will be through through real deployments in various applicative domains: electro-mobility; smart buildings; infrastructures and smart cities; industrial production; energy production and energy virtual market.

Arrowhead belongs to the first group of very large Artemis AIPP projects with an overall budget of around 90 million Euros, involving most European countries. Besides ISEP (through CISTER), the Arrowhead project involves key European industrial players such as Acciona (SP), Airbus Operations (FR), FIAT (IT), Ford (UK), Honeywell (CZ), INDRA (SP), Infineon (AT), NXP (FR), Schneider Electric (FR), STMicroelectronics (IT), and Thales (FR).

27th International Conference on Architecture of Computing Systems successfully held in Luebeck

CISTER/INESC-TEC researcher Eduardo Tovar served as Program co-chair of the 27th International Conference on Architecture of Computing Systems (ARCS 2014). The conference tool place in Luebeck, Germany, on February 25 - 28.

The ARCS series of conferences is one of the most important and oldest scientific events for computer architecture research in Europe. It celebrated this year 40 years of tradition reporting top notch results in

computer architecture , operating systems and computing systems.

The focus of the 2014 conference was on embedded computer systems connecting computing with the physical world, a topic also known as Cyber-Physical Systems. This year's highlights included a set of three high quality keynote talk, by Karl-Henrik Johansson (KTH, Sweden), Ravi Nair (IBM T. J. W Research Centre, USA) and Thomas Ludwig (German Climate Computing Centre, Germany).

February

European Center for Ubiquitous Technologies and Smart Cities

CISTER/INESC-TEC researchers Raghuraman Rangarajan and Eduardo Tovar attended the UBICITEC meeting held in Essen, Germany, last February 13, to discuss opportunities and possibilities of collaboration, especially with respect to Horizon 2020.

UBICITEC is the European Center for Ubiquitous Technologies and Smart Cities, founded on November 2012, as a continuation of the results obtained in the European Network of Excellence on cooperating Objects CONET (FP7). The main goal of UBICITEC is to establish a World-Class Center of Excellence on Smart Cities and Ubiquitous Technologies while increasing Europe's visibility in the areas of Ubiquitous Technologies, Internet of Things, Cooperating Objects and Cyber Physical Systems.

March

New highly skilled Researcher joins CISTER

CISTER/INESC-TEC has recently welcomed a new PhD member, Dorin Maxim, to its expanding international research team.

Dorin has received his Ph.D. degree in computer science in 2013 from the university of Lorraine, France after working in the renowned INRIA - Nancy Grand Est laboratory. He obtained a master degree in computer sciences (on the topic of artificial intelligence) in 2010 and a double bachelor's degree in mathematics and theoretical computer sciences in 2008, both from the Lower Danube University in Galati, Romania.

His research interests lie in the area of Real-Time Systems with particular attention to Probabilistic Analysis of Real-Time Systems. For now he will be contributing to the SMARTS (Slack management for hierarchical real-time systems in a multicore scenario) research project and will be involved in the new Artemis EMC2 project. EMC2 will start in April with CISTER/INESC-TEC teaming up with EADS, Thales, Infineon Technologies, Ericsson, BMW, Volvo, Philips Healthcare and Siemens. The Artemis EMC2 project addresses embedded multi-core systems for mixed-criticality applications in dynamic real-time environments.

CISTER to organize highly reputed Conference on Wireless Sensor Networks: EWSN 2015

CISTER/INESC-TEC will host the 12th edition of the highly reputed European Wireless Sensor Network conference (EWSN). Being one of the leading international conferences in this area, EWSN has played a prominent role in the dissemination of innovative research and provides a high quality discussion forum.

EWSN 2015 will highlight the diversity of domains that are associated to wireless sensor networks today and welcome strong contributions to the area of wireless sensor networks, broadly defined. The conference will be an opportunity to gather researchers from all over the world, working in the forefront of research in the area, and also includes demos and poster sessions where real working systems or prototypes are shown. The hosting of this event is recognition of CISTER/INESC-TEC's contribution to this field.

The conference will be held at ISEP on February 2015.

April

CISTER Participates in a New Project on Validation of Critical Systems

CISTER/INESC-TEC is a partner of the V-SIS project which has been recently approved in the framework of the System of Incentives for Research and Technological Development (SI I&DT) of the National Strategic Reference Framework (QREN).

The V-SIS (Validation of Critical Systems) project proposes to address the challenge of critical systems validation through the creation of a validation competence centre, which will tackle the landscape of change and evolution in critical systems, triggered by normative evolutions like the recent ISO26262 (automotive) and the upgrade of DO-178C (avionics).

The V-SIS project proposes working two elemental vectors (1) functional safety and (2) critical systems validation. The work will be arranged in (i) processes innovation (RAMS techniques, model based V&V, multi-criticality systems, security fault injection) and (ii) validation laboratory development.

The project is led by Critical Software and includes CISTER/INESC-TEC and the CISUC research centre of the University of Coimbra. CISTER/INESC-TEC's role will be in the embedded real-time domain, in particular in what concerns the challenges introduced by the new multicore platforms.

CISTER's PhD Student Successfully Defends His Thesis

CISTER/INESC-TEC PhD student Gurulingesh (Guru) Raravi has successfully defended his PhD thesis titled "Real-Time Scheduling on Heterogeneous Multicores". Guru received his PhD with distinction from the University of Porto where he was enrolled in the PhD program jointly

taught by CISTER/INESC-TEC and FEUP.

The main opponents where Prof. Sanjoy Baruah from the University of North Carolina, (USA) and Dr. Laurent George from the Laboratoire d'Informatique Gaspard-Monge at University of Paris-Est, France, both highly respected authorities in the field.

This work significantly enhanced the scheduling theory for heterogeneous multicores. Some of the specific problems addressed in this work, had no previous solutions and hence some of the proposed solutions in this work are first of their kind. Furthermore, for the problems where solutions existed before, the solutions proposed in this thesis are better than the existing solutions either in terms of the speedup factor or run-time complexity or average-case performance or a combination of these factors.

Throughout his work, Guru has managed to achieve recognition of his research as evidenced by the Outstanding paper award at 24th Euromicro Conference on Real-Time Systems (ECRTS 2012) and the Best paper award at 6th Junior Researcher Workshop on Real-Time Computing (JRWRTC 2012). Besides these awards, results of his work were published in several reputed conferences such as RTSS 2010, RTSS 2012, ECRTS 2012, etc. and also in journals such as Real-Time Systems Journal 2013, 2014.

After this fruitful collaboration with CISTER/INESC-TEC for the last 4 years, Guru will now join the highly reputed Xerox Research Institute in Bangalore, India.

CISTER hosts two General Assembly Meetings of European Projects

Beginning of April CISTER/INESC-TEC hosted two project General Assembly meetings, for projects ENCOURAGE and CarCode.

The ENCOURAGE General Assembly meeting has been held at CISTER/INESC-TEC on the 1st and 2nd of April. The meeting accounted the presence of 17 persons, from 9 different ENCOURAGE partners. The main objective of the meeting was mainly to deal with open issues in some work packages and to prepare for final review of the project, which will be hosted by ENEL (Italy) in November 2014.

On April 3rd and 4th, CISTER/INESC-TEC hosted the General Assembly of the CarCoDe project. The goal of the meeting was a deep analysis the current status of the project and the definition of a timeline for the near future efforts.

The ENCOURAGE project, of the FP7/ARTEMIS Embedded Computing Systems Initiative, aims to develop embedded intelligence and integration technologies that will directly optimize energy usage in buildings with renewable energy and enable active participation in the future smart grid environment.

In the ENCOURAGE project, CISTER/INESC-TEC is leader of the WP8 Work package (exploitation,

dissemination and standardization) and of the T2.3 task, responsible for defining the ENCOURAGE architecture and for the specification and development of the ENCOURAGE middleware (and in particular of its messaging system).

The CarCoDe project aims at creating a middleware for vehicular applications to let vehicles and infrastructure communicate in a seamless and efficient way, and demonstrators of the developed technology. The research methodology involves the simulations of protocols to disseminate and collect data from vehicles via both vehicle-to-vehicle (e.g.: WAVE) and infrastructure (LTE) communication, and implementation of the middleware on On Board Units (OBUs), which are embedded systems hosted on the vehicles. The early prototypes of OBUs will communicate using the most promising options for the communication technology (wi-fi and LTE).

The consortium working on CarCoDe is built of a diverse mix of 21 partners from France, Spain, Portugal and Turkey, belonging to industry and academy alike. In particular, Airbus Defense and Space, Thales, Turkcell are leading some of the main tasks of the project.

In the context of CarCoDe, CISTER/INESC-TEC is currently finalizing the architecture for both middleware and demonstrators, and in the close future it will design a system that integrates existing OBUs in LTE infrastructure. The Portuguese partners of the consortium will implement two demonstrators, one realizing online monitoring of the status of the car, and the second to facilitate the search for an available parking spot. Moreover, CISTER/INESC-TEC is developing a simulator based on ns-3 and using WAVE and LTE modules to test the communication paradigms of vehicle-to-vehicle and infrastructure communication.

General Chair of the 20th IEEE Real-Time Applications Symposium

Eduardo Tovar served as the General chair of the 20th IEEE Real-time and Embedded Technology and Applications Symposium (RTAS 2014) which was held in Berlin, Germany, April 15-17 as part of Cyber-Physical Systems Week.

Since 2008, CPS Week is the premier event on Cyber-Physical Systems joining five top conferences in one single location, covering complementary aspects of CPS and bringing together internationally leading researchers in this dynamic field with over 600 participants in this year edition. The 20% acceptance rate of RTAS is a strong indicator of its quality and continuous interest as a premier venue for real-time topics.

RTAS is the oldest of these events and this year it is celebrating its 20th anniversary. Besides the regular paper sessions on topics such as architectures, scheduling, mixed criticalities and memory management, there was also an Industrial session with 5 invitees from Daimler, ETAS, Kalray, Airbus Group (former EADS) and AbsInt which presented real-life case studies of practical application of real-time and embedded systems in industry.

The largest ICT Artemis project, EMC2, has just started

The Artemis Innovation Pilot Project EMC2 (Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments) has just started this April 2014. During the kick-off meeting, held in Munich, Germany, on 7th and 8th of April, CISTER/INESC-TEC was represented by Eduardo Tovar.

EMC2 is the largest ICT project in Europe with nearly 100 partners and a total budget of 94 Million Euros. Infineon's CEO, Mr. Reinhard Ploss and the Bavarian Ministry of Economic Affairs and Media, Energy and Technology, State Secretary, Mr. Franz Josef Pschierer were in charge of the formal opening of the project's kick-off meeting. The agenda also included talks by the Acting Executive director of ARTEMIS and the Head of BMW Research.

EMC2 starts from the observation that the field of embedded systems is undergoing a disruptive evolution, where different types of systems and components are interconnected, thus reducing the boundaries between application domains, and placing the focus on interoperability. In addition, the increasing use of multi- and many-core processors brings additional challenges to the development of critical and real-time applications, and the process of developing new systems is inefficient and expensive.

CISTER/INESC-TEC's team involved in the EMC2 project, led by Eduardo Tovar, will participate in several of the research activities, particularly in the work packages titled "Executable Application Models and Design Tools for Mixed-Critical, Multi-Core Embedded Systems", "Dynamic Runtime Environments and Services" and "Multi-core Hardware Architectures and Concepts", and also in two of the "Living Labs".

CISTER/INESC-TEC and Critical Software are also leading a use case in the area of automotive, and involved in the use case in the area of avionics, led by the Airbus Group. The project also includes other industrial and academic partners from renowned companies such as Ericsson, BMW, Airbus, Volvo, Philips Healthcare, Siemens, Thales and Infineon Technologies.

EMC2 is a direct result of the effort developed by CISTER/INESC-TEC in the last open call for research projects in the strategic ARTEMIS initiative alongside with the project DEWI (Dependable Embedded Wireless Infrastructure) which started in March 2014. Both projects focus on applicability and industry and it is expected that it will encourage potential technology transfer activities in the future.

May

New highly skilled PhD researcher joins CISTER

Sana Ullah is the most recent PhD member to join CISTER/INESC-TEC. Sana Ullah received his Ph.D. degree in Information and Communication Engineering from Inha University (South Korea) in 2011. He worked as an Assistant Professor in the College of Computer and Information Science, King Saud University, Riyadh from December 2011 to March 2014.

He currently serves as an editor for Springer Journal of Medical Systems, KSII Transaction of Internet and Information Systems (TIIS), Wiley Security and Communication Network (SCN), Journal of Internet Technology and International Journal of Autonomous and Adaptive Communications Systems (IJAACS).

Sana served as a guest editor for many top journals including Elsevier Journal of Information Science (INS), Springer Journal of Medical System (JOMS), and Springer Journal of Telecommunication Systems (TS). He also served as a co-chair/TPC member for a number of international conferences including BodyNets, IEEE PIMRC, IEEE Healthcom, IEEE Globecom, and IEEE WCNC.

He will be developing R&D on Wireless Sensor Networks and Body Area Networks for exploitable applications and systems.

CISTER hosted a distinguished seminar from Prof. Radu Marculescu

During the visit of Prof. Radu Marculescu at CISTER with the main purpose of strengthening his collaboration with the Research Center, he took the opportunity to give a presentation on "Design of Future Integrated Systems: A Cyber-physical Systems Approach". During his talk, he addressed some fundamental issues related to the modeling and optimization of power and performance of next generation of integrated systems while taking a cyber-physical approach.

Radu Marculescu is a Professor in the Dept. of Electrical and Computer Engineering at Carnegie Mellon University, USA. He received his Ph.D. in Electrical Engineering from the University of Southern California in 1998. He has received the Donald O. Pederson Best Paper Award from the IEEE Transactions of Computer-Aided Design of Integrated circuits and Systems in 2012, the Best Paper Award of IEEE Transactions on VLSI Systems in 2011 and 2005, as well as several best paper awards in major conferences in the area of design automation and multi-core design. Currently, Dr. Marculescu is the Editor-in-Chief of Foundations and Trends in Electronic Design Automation and an Associate Editor of Elsevier Journal of Nano Communication Networks. In the past, he was an Associate Editor of IEEE Trans. on Computers, IEEE Trans. on Computer-Aided Design of Circuits and Integrated Systems, ACM Trans. on Embedded Computing Systems, and

IEEE Trans. on VLSI. He has been involved in organizing several international symposia, conferences, workshops, and tutorials, as well as guest editor of special issues in archival journals and magazines. His research focuses on design methodologies and software tools for embedded systems, cyber-physical systems, and biological systems. Radu Marculescu is an IEEE Fellow.

Successful first review of European FP7 project led by CISTER

The P-SOCRATES (Parallel SOftware framework for time-CRitical mAny-core sysTEmS) project first Review Meeting was successfully held on May 15, at the venue of the Barcelona Supercomputing Center, Spain. The review meeting was held within the block review week, organized by the Complex Systems & Advanced Computing Unit of the European Commission (CNECT A3) which brought together the “Advanced Computing project cluster”: the group of FP7 projects working in the area of Advanced Computing and financed by the European Commission under ICT Call 10.

The main objective of the block review was to analyze, measure and maximize the potential and actual impact of the projects in terms of exploitation. Each project went through an autonomous review meeting, with a common all-projects workshop on impact and exploitation held on Wednesday, May 14. The P-SOCRATES review meeting focused on the achievements in the first phase of the project, which led to the successful reaching of the project first milestone. The project exploitation views were also presented in the Wednesday workshop, in a session on real-time and reliability.

P-SOCRATES

The P-SOCRATES project will research and develop new techniques for exploiting the massively parallel computation capabilities of next-generation many-core embedded platforms in a predictable way. These platforms are well positioned for intercepting the increasingly convergence of High-Performance Computing (HPC) and Embedded Computing (EC) domains need for predictable high-performance, allowing HPC and EC applications to be executed on efficient and powerful heterogeneous architectures integrating general-purpose processors with many-core computing fabrics.

P-SOCRATES is tackling this important challenge by merging leading research groups from the HPC and EC communities. The time-criticality and parallelization challenges common to both areas are addressed by proposing an integrated framework for executing workload-intensive applications with real-time requirements on top of next-generation commercial-off-the-shelf (COTS) platforms based on many-core accelerated architectures. The project is investigating new HPC techniques that fulfil real-time requirements: the main sources of indeterminism are identified, and efficient mapping and scheduling algorithms will be proposeded, along with the associated timing and schedulability analysis, to guarantee the real-time and performance requirements of the applications.

The project partners include as research institutions, besides CISTER/INESC-TEC, the Barcelona Supercomputing Centre (Spain), the University of Modena (Italy) and the Swiss Federal Institute of Technology Zurich (Switzerland). The industrial partners of the project include ATOS (Spain) and the SMEs Evidence (Italy) and Active Technologies (Italy). The project partners are supported by an industrial advisory board, which includes well-known multi-national companies including Airbus, IBM, and Honeywell.

Besides overall coordination and technical management, CISTER/INESC-TEC is also deeply involved in the parallelism to real-time activity, leading in particular the Timing and Schedulability analysis work package.

Program Co-Chair of WFCS2014

CISTER/INESC-TEC researcher Eduardo Tovar was program co-chair of the 10th IEEE Workshop on Factory Communication Systems (WFCS) held on May 5-7 in Toulouse, France. The WFCS workshop is the largest IEEE technical event specially dedicated to industrial communication systems, which aims to provide a forum for researchers, practitioners and developers to review current trends in this area and to present and discuss new ideas and new research directions.

The 2014 program included two interesting keynotes, one on on-board networks in space systems by Olivier Notebaert, Airbus Defence and Space, France, and another one on the history of industrial communication systems over the last two decades (from Fieldbus to Automation cloud) by Peter Neumann, IFAK Magdeburg, Germany.

CISTER/INESC-TEC was the organizer of the 2000 edition in Porto (http://www.hurray.isep.ipp.pt/wfcs2000/)

June

Successful Project Review Meeting of European Project Encourage

The 3rd review meeting of ENCOURAGE project, which involves the development of a reference platform for smart grids, was held in Barcelona. The review centered on the system's middleware, implemented mainly by CISTER, and on the demonstrator deployed in Terrassa University, which monitors the campus energy consumption, produces detailed report on energy usage, and publishes real-time data on Twitter regarding how users use appliances and consume energy. This latter feature implements an educative competitive game between the responsible parties for the different rooms the campus is divided into.

Arrowhead multi-workpackage meeting

From the 9th to 12th of June Luis Lino participated on the Arrowhead Multi-Workpackage Meeting, which was held in Stavanger, Norway. During this meeting all pilot-related tasks demonstrated their main achievements by showing around 15 different demo

installations running partially on existing Arrowhead technologies.

In this meeting CISTER/INESC-TEC showed a prototype of a system which applies the flex-offer concept (a kind of energy demand-response) on the control of a legacy devices, whose operation can be controlled by smart grid applications. These legacy devices can be almost any kind of electric devices which have some flexibility on the amount of energy to be consumed and on the time when that energy is consumed. Examples of these devices are washing machines, electric heater, heat-pumps, air-conditioning, etc.

The software, implemented by César Teixeira in close cooperation with Danish partners, can now be used, with the minor adaptations, on any other Arrowhead pilot that wishes to implement the flex-offer concept.

Arrowhead belongs to the first group of very large Artemis AIPP projects. It has an overall budget of around 90 million Euros, involving most European countries. Besides ISEP (through CISTER/INESC-TEC), the Arrowhead project involves key European industrial players such as Acciona (SP), Airbus Operations (FR), FIAT (IT), Ford (UK), Honeywell (CZ), INDRA (SP), Infineon (AT), NXP (FR), Schneider Electric (FR), STMicroelectronics (IT), and Thales (FR).

The Arrowhead project addresses cooperative automation and is enabled by the technology developed around the Internet of Things and Service Oriented Architectures. The project will provide a technical framework adapted to such systems. Implementation and evaluation will be through real deployments in various applicative domains: electro-mobility; smart buildings; infrastructures and smart cities; industrial production; energy production and energy virtual market.

CISTER wins fair-play team medal

Like in previous years, INESC-TEC organized last May a football tournament gathering all its researchers. CISTER/INESC-TEC researchers have been participating in this initiative since 2012.

In this year's tournament, CISTER/INESC-TEC's team - Borislav Nikolic, Christos Chrysoulas, Patrick Yomsi, João Loureiro, Hamza Ijaz, Paulo Carvalho, Hazem Ali, Raghuraman Rangarajan, Miguel Pinho and Daniel Moreira – joined the team of HasLab, another autonomous research unit associated to INESC-TEC, which was composed of Francisco Maia, Ricardo Gonçalves, Francisco Cruz, João Paulo, Tiago Jorge and Paulo Jesus. This year 8 teams attended the matches to compete for the title of Best Team of the 14th INESC-TEC Football Tournament 2014.

Although CISTER/HASLab didn't reach the title, the team was elected by the other football teams as the Fair-Play Team being awarded the respective medal. CISTER/INESC-TEC had already taken home such a medal in the 12th edition of INESC's football tournament.

EMC2 kickoff meeting

Eduardo Tovar and Pedro Souto participated in the kick-off meeting of subtask 8.2, Hybrid Avionics Integrated Architecture, of the EMC2 Artemis Project, that took place at Airbus Group premises in Munich on 27th June. In this meeting the Airbus partners presented an overview of the demonstrator and this was followed by a discussion on

how the contributions of other partners might be integrated in that demonstrator.

EMC2 (Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments, JU grant nr. 621429) aims to develop an innovative, sustainable service-oriented architecture for mixed criticality applications in dynamic and changeable real-time environments, helping the European Embedded Systems industry to maintain its leading edge position. EMC2 is a project of 97 partners of embedded industry and research from 19 European countries and Israel with an effort of about 800 person years and a total budget of about 100 million Euro.

July

Management Meeting of the TACLe COST Action

Konstantinos Bletsas represented Portugal at the TACLe ("Timing Analysis at the Code Level") COST Action Management Committee meeting in Madrid, Spain on Monday, 7th July. As Portugal's representative, CISTER is to "channel"/represent research interest in this area from Portuguese institutions.

This management meeting was mainly dedicated to budget allocation in preparation of the upcoming project year as well as to follow-up on the project-sponsored summer school. The TACLe meeting was held jointly with the main event for Worst Case Execution Time Analysis, the WCET 2014 workshop.

COST Actions are designed to create networks of researchers in Europe around a particular topic. In this particular case, it concerns code-level timing analysis and brings together researchers from key research organizations in Europe, like the Mälardalen University, Sweden, University of York, UK, or University of Saarbrücken, Germany.

Another PhD defense which received the highest distinction

CISTER/INESC-TEC PhD student Muhammad Ali Awan has successfully defended his PhD dissertation titled "Energy and Temperature Aware Real-Time Systems" in University of Porto under the supervision of Dr. Stefan M. Petters. Ali was enrolled in a doctoral program in electrical and computer engineering (PDEEC) jointly taught by CISTER/INESC-TEC and FEUP. It is the third PhD defense from CISTER in 2014 and also the third one to receive the highest distinction!

The dissertation attempts to provide energy efficient solutions and techniques to cope with the current trends in modern embedded computing systems, while closing the gap between theoretical research and practice. In particular, it focuses on operating system-level power management and exploits the available sleep states to improve on energy efficiency while mainly concentrating on leakage power dissipation. Various aspects of the system (CPU, I/O devices, thermal management etc.) have been explored for a large range of hardware platforms. The proposed solutions have lower online complexity and consider more realistic power models when compared

to the state-of-the-art approaches. Outcomes of this research have been published in many reputed international conferences such as ECRTS, RTAS, RTCSA, RTNS, SIES and ICESS. In addition to this, four more works are under submission in renowned journals.

The president of the jury was Professor Jose Alfredo Ribeiro da Silva Matos, director of Department of Electrical and Computer Engineering of the University of Porto. The two "local" reviewers were the Associate Professor Luis Miguel Pinho Almeida and the Assistant Professor Mario Jorge Rodrigues de Sousa from the Department of Electrical and Computer Engineering, also from the University of Porto, and the two "external" reviewers were the Professor Gerhard Fohler, director of Real-Time Systems group at Technische Universitat Kaiserslautern, Germany and the Associate Professor Marko Bertogna from Dipartimento di Scienze Fisiche, Informatiche e Matematiche, Universita di Modena e Reggio Eimilia, Italy. These external members are highly respected researchers in the field of Real-Time Systems.

Last but not least, Ali is now joining CISTER/INESC-TEC as a PostDoc researcher!

One more successful PhD defense

CISTER/INESC-TEC PhD student Dakshina Dasari has successfully defended her PhD thesis entitled "Timing Analysis of Real-Time Systems Considering the Contention on the Shared Interconnection Network in Multicores". Dakshina received her PhD with distinction from the University of Porto where she was enrolled in the PhD program jointly taught by CISTER/INESC-TEC and FEUP.

In her work Dakshina has studied multiple aspects of the contention problem for shared resources in multicore settings. A particular attention was given to the contention for a single shared memory bus and the potential impact of sharing that resource on the timing behavior of the applications. She has also studied other shared resources like the memory controller and the network-on-chip in modern many-core architectures. She has contributed significantly to that research domain and has developed a set of methods to augment the state-of-the-art worst-case execution time analysis techniques with the extra delay induced by these shared resources.

Dakshina has achieved solid performance throughout the four years of her PhD, with a total of four papers published in international conferences and one paper published in a renowned journal (and another one still under submission). The main opponents were Prof. Daniel Mossé from the University of Pittsburgh, (USA) and Prof. Thomas Nolte from Mälardalen University (MDH), Västerås (Sweden), both highly respected authorities in the field.

September

CISTER visited by representatives of Embraer

On September 5th, CISTER was visited by representatives of Embraer, one of the world's leading aircraft manufacturers with its headquarters in Brazil. CISTER seized the opportunity offered by this visit to organize a workshop day during which CISTER gave an overview of the projects and

international efforts in which the team is involved.

2nd CISTER Industrial workshop: CiWork 2014

CISTER has organized and hosted the 2nd Industrial workshop on Real-time and Embedded Systems CiWork 2014, on September 26th.

CiWork 2014 gathered together around 40 industry representatives and researchers to discuss the most recent advances and innovations in the area of RTES. Being an industrial workshop the focus was on the presentations by companies which presented their views and needs and case studies.

This year's edition had two keynotes, one on European Opportunities in RTES (by FCT/GPPQ), and another on Regional Opportunities for industry-academia partnerships and the main regional strategic drivers by CCDR-N. Besides the two keynotes, there was a special focus on smart Cities with a round table lead by Câmara Municipal do Porto (department of Innovation) with the participation of Freedom Grow, Inova+, Associação Porto Digital and CISTER.

During the day several companies presented their case studies, methodologies, tools and industrial challenges in the domain of aerospace (GMV), power lines automation (EFACEC) factory automation (Critical Manufacturing), smart cities (ISA) and inovation management (Inova+).

The forum also served to create and foster synergies between industry and academia.

CISTER hosted another distinguished seminar in September from Prof. Frank Mueller

Professor Frank Mueller (mueller@cs.ncsu.edu) visited CISTER and delivered a talk on "Predictability for Uni- and Multi-Core Real-Time/Cyber-Physical Systems" in order to: (1) highlight challenges and contributions in worst-case execution time analysis for real-time system considering architectural changes over time and (2) discuss future trends and open research problems.

Frank Mueller is a Professor in Computer Science and a member of multiple research centers at North Carolina State University. Previously, he held positions at Lawrence Livermore National Laboratory and Humboldt University Berlin, Germany. He received his PhD from Florida State University in 1994. He has published papers in the areas of parallel and distributed systems, embedded and real-time systems and compilers. He is a member of ACM SIGPLAN, ACM SIGBED and a senior member of the ACM and IEEE Computer Societies as well as an ACM Distinguished Scientist. He is a recipient of an NSF Career Award, an IBM Faculty Award, a Google Research Award and a Fellowship from the Humboldt Foundation.

Final results of the BIC students (interns) at CISTER

Three pairs of enthusiastic BIC students from ISEP and FEUP joined CISTER for a three months internship program. During this time frame, they contributed to a set of very challenging projects (recalled below) under the supervision of CISTER researchers.

The presentation of their remarkable results is available at: www.cister.isep.ipp.pt/events/871/

Project 1: Sensing in motion: by Marco Rodrigues (ISEP) and Miguel Sandim (FEUP) oriented by Raghuraman Rangarajan and Vikram Gupta

Real-time environment monitoring is required to quickly address issues of pollution of noise, air, water and land. This is especially important in an urban scenario for situational awareness and improved decision making. Current air pollutant sensors are in fixed locations and away from critical places. The aim of this project is to make a modular UV-based system capable of autonomously taking environmental measurements at different localities and transmit this data in real-time.

Project 2: Vision feedback to control 3D motion: by Dalila Lima (FEUP) and Nuno Almeida (ISEP) oriented by Filipe Pacheco and Shashank Gaur

Quadcopters provide easy and affordable 3D movement capabilities and enable new robotic tasks. However controlling the position in space of a device with adequate accuracy is a challenge. In this project computer vision is used to provide real-time position feedback and enable simple control in the 3D space of the quadcopter. The target application is an plotter-like demonstration where the quadcopter can draw paths on a vertical wall without human assistance.

Project 3: Tele-presence robot: by João Pacheco (ISEP) and Paula Fortuna (FEUP) oriented by Pedro Souto and Ricardo Severino

Conventional video-conference systems although very useful allow for limited interaction. This project will combine a video-conference system with a wifibot to allow for a more interactive experience. Its goal being to allow a user to roam around a remote place and interact with remote users via a video-conference system, e.g. to remotely assist in lab work.

October

CISTER-lead European project P-SOCRATES meets in Porto

On September 30th/October 1st, the partners of the European Project P-SOCRATES gathered at CISTER, for two days of intensive technical work. This included in-depth discussions of the scientific and technical work being carried in the project work packages, but important, the specification of the holistic system model and software stack, which will be presented for the 2nd milestone of the project, in the first quarter of 2015. The partners also evaluated the detailed feedback received by the commission on the contents of the first review, which provided very positive remarks on the work being developed, confirming the relevance of the foreseen objectives, as well as stressing the capability and importance of innovation and exploitation.

The P-SOCRATES project is researching and developing new techniques for exploiting the massively parallel computation capabilities of next-generation many-core embedded platforms in a predictable way. These platforms are well positioned for intercepting the increasingly convergence of High-Performance Computing (HPC) and Embedded

Computing (EC) domains need for predictable high-performance, allowing HPC and EC applications to be executed on efficient and powerful heterogeneous architectures integrating general-purpose processors with many-core computing fabrics.

The project partners include as research institutions, besides CISTER/INESC-TEC, the Barcelona Supercomputing Centre (Spain), the University of Modena (Italy) and the Swiss Federal Institute of Technology Zurich (Switzerland). The industrial partners of the project include ATOS (Spain) and the SMEs Evidence (Italy) and Active Technologies (Italy). The project partners are supported by an industrial advisory board, which includes well-known multi-national companies including Airbus, IBM, and Honeywell.

Besides overall coordination and technical management, CISTER/INESC-TEC is also deeply involved in the parallelism to real-time activity, leading in particular the Timing and Schedulability analysis work package.

Horizon 2020 Infoday

CISTER Researcher Luis Miguel Pinho represented the research centre in the ICT Proposers' Day 2014, an event that took place in Florence, Italy on 9th and 10th October 2014 to promote European ICT Research & Innovation, focusing on the Horizon 2020 Work Programme for 2015, in the field of Information & Communication Technologies.

This event offered an exceptional opportunity to build quality partnerships as it connected academia, research institutes, industrial stakeholders, SMEs and government actors from all over Europe. More than 2000 participants discussed the 2015 ICT project calls, including topics in Leadership in Enabling and Industrial Technologies, such as low-power embedded computing, robotics, big data research, and in Societal Changes, such as health and wellbeing, energy efficiency and smart cities.

CISTER is currently involved in several initiatives targeting some of the calls of the 2015 work program, both for Research and Innovation Actions, following the path of current CISTER scientific activities, as well as larger Innovation Actions, where some of CISTER past research results is integrated.

New researcher joins CISTER

Maria Ángeles Serna recently joined CISTER as a post-doc researcher. Maria received a B.Sc. degree in Computer Science in 2008, a M.Sc. degree in Advanced Computer Technologies in 2010, and a PhD degree in Computer Science with honors ("cum laude") in 2013, all both from the University of Castilla-La Mancha. She was a postdoctoral researcher in the Department of Computer Science, University College Cork between July 2013 and June 2014.

Previous to the start of her PhD studies, Maria held a position as a developer in a private company, implementing Geographic Information Systems. She also held several positions as a developer at University Castilla-La Mancha. During her PhD studies, Maria was also a visiting researcher at CISTER/INESC-TEC.

Her research interests include collaborative processing of environmental information in wireless sensor networks, including data

dissemination techniques, phenomena monitoring, modeling and simulation.

Another PhD from CISTER's ranks

CISTER Researcher Vikram Gupta successfully defended his PhD thesis at the Carnegie Mellon University, Pittsburgh, USA, on Oct 13th 2014, under the Carnegie Mellon-Portugal dual PhD program. The thesis, entitled "On the Optimization of Multiple Applications for Sensor Networks", was supervised by Prof. Eduardo Tovar (CISTER/INESC-TEC) and Prof. Raj Rajkumar (CMU). The committee was also composed by Prof. Peter Steenkiste (CMU), Prof. Anthony Rowe (CMU) and Prof. José Silva Matos (FEUP).

For Vikram, this was a the pinnacle of a research path developed between Pittsburgh and Porto in the past 6 years, during which a number of seminal results were published in top-venues in the area of real-time embedded systems and wireless sensor networks, including a best paper award at the prestigious ACM SenSys conference.

CISTER researchers chair the 8th Junior Researcher Workshop on Real-Time Computing (JRWRTC)

This year, the junior workshop JRWRTC traditionally organized in conjunction with the 22nd International Conference on Real-Time and Network Systems (RTNS), has been chaired by two researchers of CISTER: Geoffrey Nelissen and Dorin Maxim. The workshop took place in Versailles on the 8th of October and was a success with 13 short papers of 4 pages presented.

The purpose of this 8th Junior Researcher Workshop on Real-Time Computing (JRWRTC) is to bring together junior researchers working on real-time systems (PhD students, postdocs, etc.). It provides a relaxed forum to present and discuss new ideas, new research directions, and to review current trends in this area. The workshop is based on short presentations and a poster session that encourage discussion by the conference attendees.

The award for the best paper of the workshop (a Nexus 7) has been given to Remy Boutonnet and Mihail Asavoae for their paper titled "The WCET Analysis using Counters - A Preliminary Assessment".

Largest European R&D project in the area of wireless sensor networks and wireless communication visits Porto

More than 70 DEWI project partners attended a successful official meeting on 27–29 October 2014, hosted by CISTER in Porto, Portugal.

Besides dedicated work meetings related to the technical work being developed in the project, the members of the main DEWI governance boards (Technical Board, Steering Board, General Assembly) have met to debate DEWI overall status and technical progress, requirements management and other relevant specific topics.

CISTER researchers had a strong contribution for the work in this meeting and in DEWI so far. CISTER is the leader of the application domain on aeronautics, and also leader of the technical board, one of the main governance bodies of DEWI.

November

High participation of CISTER in ECSEL JU Calls

CISTER has successfully participated in the recent ECSEL JU calls and participated in the submission of nine proposals. The proposals are on various CPS-related topics including, smart city infrastructure and applications, safety assurance, security, maintenance and testing. CISTER's intended research contributions include issues in runtime monitoring, timing, schedulability, verification and testing, communication, security, middleware and various pilot demonstrators.

CISTER participates in H2020 project EnergAware accepted in highly competitive call

In the scope of the European R&D program H2020, in the topic "New ICT-based solutions for energy efficiency", CISTER participates in the project proposal EnerGAware (Energy Game for Awareness of energy efficiency in social housing communities), which has been recently selected for a grant.

The topic "New ICT-based solutions for energy efficiency" intends to motivate and support citizen's behavioural change to achieve greater energy efficiency taking advantage of ICT (e.g. personalised data driven applications, gaming and social networking) while ensuring energy savings from this new ICT-enabled solutions are greater than the cost for the provision of the services. This was a highly competitive call, with only 4 projects approved out of 94 submitted proposals.

The EnergAware project intends to achieve a 15-30% energy consumption and emissions reduction in a social housing pilot and increase the social tenants' understanding and engagement in energy efficiency through the development of a serious game that will be linked to the actual energy consumption (smart meter data) of the game user's home and embedded in social media and networking tools.

The project is led by the Group of Construction Research and Innovation of the Universitat Politècnica de Catalunya, Spain, including also as partners the game developer Fremen Corp, France, the embedded platform provider Advantic SIS, Spain, the Building Performance Analysis and Sustainability & Psychology groups of the Plymouth University, UK, the Devon and Cornwall social housing provider, UK, and the EDF Energy R&D UK Centre, UK.

CISTER will be involved in several of the activities of the project, being in particular responsible for the design and implementation of both the data collection infrastructure, and the middleware performing real-time data management. CISTER will also lead the work package on the integration of the data collection and communication platform and the EnerGAware game.

Two talented PhD candidates joined CISTER/INESC-TEC

The CISTER/INESC-TEC Research Unit (http://www.cister.isep.ipp.pt/) recently announced two PhD candidate positions in Electrical and Computer Engineering with 3-4 year grants, starting in November 2014.

In response to this call, a total of around 68 applications were received from four continents (Europe, Asia, America and Africa). These applications went through a rigorous three-stage review process and finally two candidates were selected. Research grants will be provided to the selected PhD candidates for up to four years with 12.000,00 € (after taxes) salary per year (the standard value of FCT's PhD grants).

Invited seminar in one of the leading research labs in Europe

CISTER Researcher Konstantinos Bletsas had the honor to present 3 seminars at one of the leading labs in the area, the ReTis Lab, in Pisa (04-06/11/2014), by invitation from Prof. Buttazzo, two on semi-partitioned multiprocessor scheduling and one on WCET analysis for GPUs . These seminars counted towards the course requirements of PhD research students.

The first two seminars were on semi-partitioned multiprocessor scheduling (respectively, the families of slot-based and timed-migration-based algorithms). The last seminar covered approaches for the WCET analysis for GPUs (including the work done by CISTER PHD student Kos Berezovskyi).

Besides the great hospitality, as part of this visit, Konstantinos had interesting discussions and interactions with the lab members for the purpose of identifying topics for potential collaboration. Seminal ideas that can foster follow up joint research were discussed and concrete proposals might sparkle out of those.

December

Towards the second milestone of P-SOCRATES

On December 5th, the partners of the European project P-SOCRATES gathered for a one-day technical meeting in Rome, Italy. The participants made significant progress in clarifying the specifics of the system model and software stack that will be presented to the reviewers at the 2nd milestone of the project, in the first quarter of 2015. The partners also evaluated their individual exploitation plan and discussed the deliverable on exploitation.

The P-SOCRATES project is researching and developing new techniques for exploiting the massively parallel computation capabilities of next-generation many-core embedded platforms in a predictable way. The project partners include the research institutions Barcelona Supercomputing Centre (Spain), University of Modena (Italy) and Swiss Federal Institute of Technology Zurich (Switzerland). The industrial partners include ATOS (Spain), Evidence (Italy) and Active Technologies (Italy). The project partners are supported by an industrial advisory board, which includes well-known multinational companies including Airbus, IBM, and Honeywell.

Besides overall coordination and technical management, CISTER/INESC-TEC is also deeply involved in the parallelism to real-time activity, leading in particular the Timing and Schedulability analysis work package.

A new visiting scholar for CISTER

Damien Masson, an associate professor in the Systems Engineering department (ISYS) of ESIEE Paris - a founding member of Université Paris-Est - is joining CISTER/INESC-TEC as a visiting scholar until June 2015.

Damien defended a PhD thesis on Real-Time systems in December 2008 entitled: "Non periodic events integration in real-time systems: application to the event management in the Real-Time Specification for Java". He is interested in all research topics related to real-time scheduling.

During his stay at CISTER he will be working on Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments. Damien is also a member of the Gaspard-Monge computer science research laboratory (LIGM) in the LRT team.

CISTER advances its smart city initiatives

Smart cities have become an important narrative for using technologies to improve quality of life, especially in urban scenarios. CISTER has already started furthering its contributions in this area and recently participated in a number of networking events, namely the Smart City Expo in Barcelona and UBICITEC an European Center with the objective of establishing a world-class center of excellence on smart cities and ubiquitous technologies.

These visits focused on networking with like-minded institutions and individuals working in the field, and understanding the issues being tackled around the world in the form of experiences and case studies.

In an important development, Eduardo Tovar has been elected for the Steering Committee of UBICITEC for the year 2015 together with Prof, Jose Marron (U. Dessen, Germany) and Antonio Moreno (ETRA I+D, Spain)

CISTER is collaborating with the Câmara Municipal de Porto, a leading player to make Porto one of the European smart cities on various joint project proposals addressing several issues in this area. CISTER will also organize a workshop related to smart city during EWSN 2015 that will bring together leading experts and participants from various allied domains.

ECSEL project proposal enters negotiation phase

The European research project proposal MANTIS submitted to the last ECSEL JU call was approved and passed to the negotiation phase.

The overall concept of MANTIS (Cyber Physical System based Proactive Collaborative Maintenance) is to provide a proactive maintenance service platform architecture based on Cyber Physical Systems that allows to estimate future performance, to predict and prevent imminent failures and to schedule proactive maintenance. The research addressed in MANTIS will contribute to companies' assets availability, competitiveness, growth and sustainability. Use cases will be the testing ground for the innovative functionalities of the proactive maintenance service platform architecture and for its future exploitation in the industrial world. Results of MANTIS can be utilized directly in several industry areas and different fields of maintenance.

CISTER/INESC-TEC will be part of a Portuguese consortium integrating INESC-TEC, UNINOVA and ADIRA. In this project CISTER/INESC-TEC will lead the work package related to dissemination and will work on an industrial pilot using ADIRA machines and also on the development of sensors for maintenance, their communication protocols and the middlewares which will make that information available to higher layers.

The ARTEMIS Joint Undertaking (which is now part of ECSEL) has always been one of the flagship and most attractive funding frameworks that has fostered scientific research in Europe, in particular the research in cyber-physical systems. Throughout the years researchers in CISTER/INESC-TEC have been active members of numerous project consortium with a successful track record of accepted projects at every call. CISTER perpetuated this tradition with the MANTIS project.

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3. Raravi, G, "Real-Time Scheduling on Heterogeneous Multiprocessors", PhD Thesis. 17, Mar, 2014. Porto, Portugal.
4. Gupta, V, "On the Optimization of Multiple Applications for Sensor Networks", PhD Thesis. 2014. Pittsburgh.

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59. Pinho, L, Bertogna, M, Quiñones, E, Benini, L, Carlos, J, Ramponi, M, Scordino, C, "Time Criticality Challenge in the Presence of Parallelised Execution", 2nd Workshop on High-performance and Real-time Embedded Systems (HiRES 2014). 20, Jan, 2014. Vienna, Austria.
60. Nikolic, B, Yomsi, P, Petters, S, "Worst-Case Communication Delay Analysis for Many-Cores using a Limited Migrative Model", 20th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2014). 2014, Real-Time Systems Track. Chongqing, China.Italy.

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61. Baldovin, A, Zovi, A, Tovar, E, Nelissen, G, Vardanega, T, "Modelling Avionics Applications with CONCERTO", Demo in RTSS@Work 2014 -Open Demo Session of Real-Time Systems, IEEE Real-Time Systems Symposium (RTSS 2014). 2 to 5, Dec, 2014. Rome, Italy.
62. Nélis, V, Yomsi, P, Pinho, L, Bernat, G, "Another look at the pWCET estimation problem", Poster presented in Work in Progress Session, IEEE Real-Time System Symposium, Work-in-progress session, 2014 (RTSS 2014). 2 to 5, Dec, 2014. Roma, Italy.
63. Esper, A, Tovar, E, "Resource Sharing Under a Server-based Semi Partitioned Scheduling Approach", Poster presented in 22nd International Conference on Real-Time Networks and Systems (RTNS 2014). 8 to 10, Oct, 2014. Versailles, France.
64. Pinho, L, Marín_Carrión, I, Ferreira, L, "On Program Restructuring for Cluster-based Highly Parallel Embedded Architectures", Poster presented in INFORUM - Simpósio de Informática (INFORUM 2014). 4 to 5, Sep, 2014. Porto, Portugal.
65. Robles, R, "Order statistics of exponential random variables with imperfect measurement and unknown Gaussian disturbance for resource allocation compression models", Poster presented in UCL-Duke Workshop on Sensing and Analysis of High-Dimensional Data. 4 to 5, Sep, 2014. London, United Kingdom.
66. Gupta, V, Pereira, N, Tovar, E, Rajkumar, R, "A Harmony of Sensors: Achieving Determinism in Multi-Application Sensor Networks", Poster presented in 13th ACM/IEEE International Conference on Information Processing in Sensor Networks (IPSN'14). 15 to 17, Apr, 2014, pp 299-300. Berlin, Germany.

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67. Fotouhi, H, Moreira, D, Alves, M, "Mobile IoT: smart-HOP over RPL", 16, Jul, 2014.
68. Fotouhi, H, Alves, M, Zuniga, M, Koubâa, A, "Reliable and fast hand-offs in low-power wireless networks (extended paper)", 14, Feb, 2014.
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People

www.cister.isep.ipp.pt/people

Åkesson, Benny

PhD Eindhoven University of Technology, Netherlands

Research Associate

Benny Åkesson was born in Landskrona, Sweden in 1977. He earned a M.Sc. degree in Computer Science and Engineering at Lund Institute of Technology, Sweden in 2005. In 2010, he received his Ph.D. degree in Electrical Engineering at Eindhoven University of Technology, the Netherlands, on the topic of "Predictable and Composable SoC Memory Controllers". This research was conducted in collaboration with NXP Semiconductors. Prior to joining the CISTER research unit, Dr. Åkesson worked as Postdoctoral Researcher and Assistant Professor at the Eindhoven University of Technology, where he is led the memory research team in the Electronic Systems group at the faculty of Electrical Engineering. His primary research interests include memory controller architectures, real-time resource scheduling, performance modeling, and virtualization. He is the author of a book about memory controllers for real-time embedded systems.

Albano, Michele

PhD University of Pisa, Italy

Research Associate

Michele Albano received his BSc degree in Physics in 2003, and his BSc, MSc and PhD degrees in Computer Science in 2004, 2006 and 2010 respectively, all of them from the University of Pisa, Italy. He was visiting researcher at Universidad de Malaga (Spain) in 2007, at Stony Brook University (New York, USA) in 2009, and before being a researcher he worked as software engineer and wireless technology specialist in private companies in the period 2001-2006, and he founded an SME. In 2006 and 2007 he was involved in EU funded projects SMEPP and XtreemOs, and in the period 2010-2012 he held a post-doctoral researcher position at the Instituto de Telecomunicações (Portugal), He is currently a Research Scientist in the CISTER and has published the book "Data Centric Storage in Wireless Sensor Networks: Advanced Techniques". His main research interests are in the areas of wireless sensor networks, energy saving in wireless communication, and peer-to-peer networks.

Al-Asadi, Amine

Technical Staff, Administrative Support

Amine Al-Asadi joined the Cister Research Unit in September 2011. She is part of our technical support staff and assists the group in organizational matters as well as administrative work.

Ali, Kiran

MSc Student

Kiran Ali got her first degree in Computer Science from Gomal University, Dera Ismail Khan, Pakistan. Currently, she is pursuing a Master's in Computer Science with specialization in Parallel and Distributed Systems from University of Porto, Portugal. Her area of interest is Parallel and Distributed Embedded Systems.

Ali, Hazem

PhD Student

Hazem completed his MSc in Embedded and Intelligent Systems at the School of Information Science of the Halmstad University, Sweden, September 2010. He is currently doing his PhD at CISTER in the area of real-time languages.

Alkhawaja, Abdel Rahman

PhD Student

Abdel Rahman received his bachelor degree in Computer Engineering form University of Jordan in 2006 and completed his master in Computer Network Engineering in Halmstad University, Sweden, 2011. He has previously worked in network operation center.
His research interests are wireless sensor networks, mobile communication system and networking. Currently, he is doing his PhD at CISTER Research Unit.

Almeida, Inês

Administrative Assistant

Inês Almeida used to live in Brussels where she worked as a professional contemporary performer. Four years ago she came back to her origins and got her degree in Administrative Assistance and Translation from the Administration and Accountancy School of the Polytechnic Institute of Porto. Currently, she is pursuing a Master's in Innovation and Technological Entrepreneurship at the Faculty of Engineering of the University of Porto, Portugal.

Almeida, Sandra

Management Support

Sandra Almeida joined the group in 2002. She is the Financial & Administrative Manager. She got a degree in Management Assessorship, from the Polytechnic Institute of Porto, School of Accounting and Administration.

Almeida, Nuno

Undergrad Student

Nuno Almeida was born in 1994 and he's studying Computer Science in Polytechnic Institute of Porto. He also is finishing a small Photoshop course. He has various interests, all in the computer science region, like Game Development, Graphic Design, Parallel Computing and programming in general.

Alves, Mário

PhD University of Porto, Portugal

Professor, Research Associate

Mário Alves was born in 1968 and has a Degree (1991), a MSc (1995) and a PhD (2003) in Electrical and Computer Engineering at the University of Porto, Portugal. He is a Professor in ECE at the Polytechnic Institute of Porto (ISEP/IPP) and a Research Associate and Wireless Sensor Networks (WSNs) research line leader at CISTER. He has been actively participating in the organization of several international conferences and workshops (e.g. EWSN, ECRTS, IEEE WFCS, CONET). His personal research interests are mainly devoted to supporting quality-of-service (QoS) in large-scale and dense WSNs, mainly based on standard and COTS technology. He is currently involved in several national and international projects and networks of excellence. The WSN team at CISTER has been attaining many important achievements and international visibility, such as 1) deploying the largest WSN test-bed in Europe so far (300+ nodes, under the EMMON project); 2) scoring over 115000 visits and 6000 downloads of the open-ZB toolset; and 3) being founding members of and active contributors to the TinyOS 15.4 and ZigBee Working Groups.

Awan. Muhammad Ali

PhD Student

Muhammad Ali Awan did his master's Degree from Royal Institute of Technology(KTH) Sweden in System on Chip Design with a focus on Digital System Design and Embedded Systems. He worked as Lecturer in National University of Science and Technology Pakistan. He also worked as a researcher in IMEC, Belgium for two years. His research focus was on High Level Memory Management. Currently he started his PhD in Cister and participating in a research on "Real-Time Power Management on Partitioned Multicores".

Baldovin, Andrea

Visiting PhD Student

Andrea Baldovin is a PhD student in Computer Science at the University of Padua. He received his Bachelor's and Master's Degree from the same institution, where he has been involved in the EU-FP6 SPADE project and in the EU-FP7 PROARTIS project. His research interests include Worst-Case Execution Time (WCET) Analysis of hard real-time systems, with particular attention to time-composable architectures and real-time operating systems.

Barros, Cristiana

Administrative Assistant

Cristiana Barros was born and raised in the town of Chaves. In 2003 she moved to Oporto to study Communication, Public Relations, Advertising and Marketing; from an early age she developed an interest in the audiovisual area, having her first audiovisual experience as Second Assistant Director in 2006, in the short film "Área Protegida" by José Miguel Moreira.
She has worked along with Paulo Calheiros as her assistent making her first steps into photography. Currently she is attending a degree in Audiovisual and Multimedia Communication and working as a freelancer photographer.

Barros, António

Lecturer, PhD Student

António Manuel de Sousa Barros was born in 1974 and has a 5 year degree (1997) and a master degree in Electrical and Computer Engineering at the Universtity of Porto.Since 2001 he has been a teacher assistant at the Department of Computer Engineering. He was researcher at the Biomedical Engineering Institute (University of Porto) from 1998 to 2001. He also worked as freelancer in the fields of electronics and computer programming. Since January 2005 he is also with the CISTER.His interests are in real-time telecommunication systems and reliable software.

Berezovskyi, Kostiantyn

PhD Student

Kostiantyn Berezovskyi holds M.Sc. degree from Taras Shevchenko National University of Kyiv. At university he paid great attention to software development and have gathered experience in parallel programming. Now he is a PhD student at CISTER. His interests are related to the schedulability analysis of general purpose graphics processor units.

Bletsas, Konstantinos

PhD University of York, United Kingdom

Research Associate

Konstantinos Bletsas (born in 1978 in Greece) has a Degree in Electronic and Computer Engineering (2002) from the Technical University of Crete (Chania, Greece) and a PhD in Computer Science (2007) from the University of York (UK). His PhD was about the response time analysis of hard real-time systems with application-specific co-processors. He joined the group in 2007 to do research on multiprocessor scheduling algorithms.

Burmyakov, Artem

PhD Student

Artem Burmyakov received a masters' degree in Computer Sciences from Moscow Engineering and Physics Institute. He worked as a software engineer within CERN for more than 4 years, participating in the LHC GCS and the UAB projects. Nowdays he is a doctoral student within CISTER. His professional interests are related to the development of control, real-time and distributed systems.

Carvalho, Paulo

Technical Staff

Paulo David Peixoto de Carvalho (born in 1993 in Miragaia, Porto) graduated in Electronic, Automation and Computers in Escola Profissional de Tecnologia e Electrónica (ESTEL). At its Professional Aptitude Test (PAP) he presented a Home
Automation controlled by programming in Visual Basic 2010 and CX-Programmer, working from an automaton CP1L. Since finishing the course (2011) he had the opportunity to work in the field of automotive painting and as a telecommunications sales technician.
He is currently working at CISTER/INESC-TEC providing support for the operation and maintenance of equipment and infrastructure.

Castanho, Francisco

MSc Student

Francisco Castanho was born in 1989 and has a bachelor's degree(2012) in Informatics engineering by the School of Engineering, Polytechnic Institute of Oporto. Currently he is developing his Master's Thesis at CISTER. His main interests are real-time systems, multi-processor scheduling algorithms, and safety-systems.

Chrysoulas, Christos

PhD University of Patras, Greece

Research Associate

Christos Chrysoulas received his PhD in Electrical & Computer Engineering from the Electrical & Computer Engineering Dept., University of Patras, Greece in 2009. He received his Diploma in Electrical & Computer Engineering from the Electrical & Computer Engineering Dept., University of Patras, Greece in 2003. Since then he is working as an Adjunct Professor, in the Technological Educational Institute of Patras, Hellas. His research interests include Computer Networks, High Performance Communication Subsystems Architecture and Implementation, Wireless Networks, New Generation Networks Architectures, Resource Management and Dynamic Service Deployment in New Generation Networks and Communication Networks, Grid Architecture, Semantics.

Dasari, Dakshina

PhD Student

Dakshina Dasari was born in 1980 in India. She has a Bachelors Degree from Karnataka University Dharwad and finished her Masters in 2004 from National Institute of Technology, Surathkal (NITK), India. She has five years of working experience - 3 yrs at Sun Microsystems and 2 yrs at Citrix Pvt Ltd as Software Engineer. She has previously worked in the area of Networking.

Duarte, Roberto

Undergrad Student

Roberto Daniel Alves Duarte was born on 1988. He is in the third year of a Bachelor degree in Informatics engineering by the School of Engineering, Polytechnic Institute of Oporto. Currently he is developing his bachelor's internship at CISTER. His main interests are Adaptive RT Systems, RT Software and Multi-core Systems.

Dumez, Thomas

Undergrad Student

Thomas Dumez was born in Liège, Belgium, in 1986. He is in the third year of a Bachelor degree in Industrial Computer Science at "Haute Ecole de la Province de Liège (Belgium)". To complete his studies, he decided to do an Erasmus in Porto and join CISTER Research Unit where he is studying the topic "Implementation of a work-stealing scheduler in a real-time operating system".
During his curriculum, he has studied several subjects from which the following are highlighted: real-time operating systems, real-time programming (POSIX 1003.1b), embedded systems, robotics and microprocessor architectures.

Easwaran, Arvind

PhD University of Pennsylvania, U.S.A.

Research Associate

Arvind Easwaran was born in Mumbai (formerly Bombay), India, in 1979. In 2001 he graduated with a Bachelor of Engineering (BE) in Computer Engineering from Mumbai University, India. After that he had a brief stint first at the Indian Institute of Technology (IIT), Bombay, as a Project Engineer with Prof. Subramani Arunkumar, and then at Infosys Technologies Ltd. as a Software Engineer. In 2005 he was awarded the Master of Science in Engineering (MSE) degree, and in 2008 he was awarded the Doctor of Philosophy (PhD) degree, both in Computer and Information Science from the University of Pennsylvania, USA. His academic advisors were Prof. Insup Lee and Prof. Oleg Sokolsky. During PhD studies, he also had a brief stint at Honeywell, Advanced Technology, as a research intern. Since January 2009, he has been working at CISTER as a research scientist in the area of real-time scheduling theory.

Esper, Alexandre

PhD Student (Industry)

Alexandre Esper was born in 1974, in the state of São Paulo, Brazil. He holds a degree (1998) in Electrical Engineering from the State University of Campinas, Brazil, and a Master of Space Systems Engineering (2011) from the Delft University of Technology, in the Netherlands.

Mr. Esper is an experienced system and software engineer (+15 years). He has been working as a senior engineer and technical manager at Critical Software S.A. since 2005 in projects for the aerospace sector, mainly in ESA missions, such as: Sentinel-3, Sentinel-1, Herschel-Planck, GOCE, Lisa Pathfinder, GAIA, VEGA launcher. His expertise includes spacecraft subsystems (mainly on-board computer hardware and software), ground segment system and software (mainly SCOS-2000) and launchers (mainly on-board computer hardware and software).

Before joining Critical Software, Mr. Esper worked as a mobile systems engineer for NEC from 1998 to 2005, including projects in NEC Brazil, NEC UK and NEC Portugal. He became an expert in mobile network optimization and planning, protocol analysis, interoperability testing (IOT), conformance testing, software validation and product validation.

Ferreira, Luis Lino

PhD University of Porto, Portugal

Professor, Research Associate

Luis Lino Ferreira was born in 1971 and has a MSc (1997) and a PhD (2005) in Electrical and Computer Engineering at the University of Porto. Since 1996 he works as a professor at the Department of Computer Engineering, School of Engineering of the Polytechnic Institute of Porto. He was a researcher at the Systems and Robotics Institute, Industrial Automation Group (University of Porto), from 1994 to 1996, in the area of Real-Time Control Systems. Since 1997 he is a member of the IPP-HURRAY research group, where he is currently working on Wireless and mobile networks.

Fonseca, José

PhD Student

José Carlos Fonseca was born in 1987, in Porto, Portugal. He holds a BSc (2010) and a MSc (2012) both in Computer Engineering from the School of Engineering of the Polytechnic Institute of Porto (ISEP). Currently, José is pursuing a PhD in Electrical and Computer Engineering at the University of Porto. Since he joined CISTER Research Unit in February 2012, his main research interests are in real-time operating systems and scheduling theory for multi- and many-core platforms.

Fortuna, Paula

Undergrad Student

Paula Fortuna, is an undergraduate student of the Informatics and Computing Engineering Masters at FEUP. Her main research interests include low-level programming and algorithm analysis.

Fotouhi, Hossein

PhD Student

Hossein Fotouhi received his degree on Electrical Electronics Engineering in 2004 and worked afterwards about three years in Iran in different places such as University of Guilan and Telecommunication Center as a network engineer. He obtained his Master of Science in Communication Network Engineering in 2009 from University Putra Malaysia. His MSc thesis was on "optimizing energy consumption in MAC layer for Wireless Sensor Networks"Currently, he is doing his PhD research in CISTER Research Unit since July 2009. His research interests are wireless sensor networks, mobility management, handoff mechanism and fuzzy logic theory.

Garibay-Martínez, Ricardo

PhD Student

Ricardo Garibay-Martínez was born on 1984 in Morelia, Mexico. Ricardo received his Bachelors Degree from Morelia Institute of Technology (ITM) in 2007 and finished his Master of Science in Computer Science from Centre for Scientific Research and Higher Education of Ensenada (CICESE), Mexico. He has experience working as a lecturer and as a researcher for PEMEX Petroleum Company. Since 2007, he has been working in the area of Adaptive Resource Management in Distributed Dynamic Real-Time Systems.Currently, he is working as a researcher and PhD student in CISTER/IPP-HURRAY Research unit. His current research interests are Adaptive RT Systems, RT Software and Multi-core Systems.

Gaur, Shashank

PhD Student

Shahsank Gaur is a recent graduate from ECE Paris in Embedded System. His research interest are Wireless Sensor networks, Software Defined Radio, etc. He has extensively worked on various industrial and research projects in past with organizations such as GNURadio, EADS, Infineon Technologies, Ansaldo STS(Finmeccanica Group), Aldebaran Robotics, etc.Before graduating from ECE Paris, he completed undergraduate studies in Electronics and Communications from BKBIET, Pilani, India in 2011.

Gupta, Vikram

PhD Student

Vikram Gupta is a PhD candidate in Electrical and Computer Engineering in the Carnegie Mellon University (CMU) - Portugal joint program beginning August 2008 and is supervised by Prof. Raj Rajkumar (ECE-CMU) and Prof. Eduardo Tovar (ISEP-IPP). His current research includes developing clock synchronization methods for Wireless Sensor Networks. Before joining PhD program, he was working as a research associate at Indian Institute of Technology (I.I.T.) Delhi, India, where he focussed on Performance Assessment and Interoperability of WiMAX (802.16) on a Campus based Test Bed. He received his degree of Bachelor of Technology from National Institute of Technology (V.N.I.T.) Nagpur India in May 2007.

Ijaz, Hamza

Junior Researcher

Hamza Ijaz has a master's in Design and Implementation of ICT Products and Systems from Royal Institute of Technology(KTH) Sweden and a bachelor's in Electrical and Computer Engineering from Center for Advanced Studies in Engineering(CASE) Pakistan. Hamza has worked in research and development projects addressing various aspects of embedded and electronics systems.His main areas of interest are embedded systems, sensor based systems, high speed digital design and machine vision.

Koubâa, Anis

PhD Nat. Polytechnic Institute/INPL, France

Professor, Research Associate

Anis KOUBÂA was born in 1977 in Tunisia and has an Engineering Degree in Telecommunications (2000) from Sup'Com (Tunisia), a Master Degree in Computer Science (2001) from University of Nancy I (France), and a PhD in Computer Science (2004) from National Polytechnic Institute (INPL). His PhD work addressed the definition and analysis of graceful degradation of real-time quality of service in guaranteed-rate Networks using (m,k)-firm model. From March 2005, he is involved in a post-doc project on Real-Time Communication in Wireless Sensor Networks at CISTER research group. His main research activities focus on real-time, quality of service and wireless sensor networks. His Post-Doctoral work in CISTER is focused on Wireless Sensor Networks with an emphasis on real-time aspects.

Kurunathan, Harrison

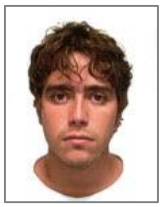
PhD Student

John Harrison Kurunathan received his degree in Electronics and Communication Engineering from SRM University in the year 2012. He obtained his Masters in engineering in the field of very large scale integrated systems from SSN College of Engineering in the year 2014. He has worked in the research unit of SSN College of Engineering.
He is currently enrolled in the PDEEC doctoral program in the University of Porto.
His current research interests are Embedded Systems, Robotics and Micro electro mechanical systems.

Lima, Dalila

Undergrad Student

Dalila Lima is currently taking a degree in Informatics and Computing Engineering at Faculdade de Engenharia da Universidade do Porto. Her main interests are Information Security, Networks, Low-level Programming and Data Mining.



Loureiro, João

PhD Student

João Loureiro holds a degree in Mechatronic Engineer since 2009 from Pontifícia Universidade Católica de Minas Gerais, Brazil. He has worked in research and development of embedded systems, both inside industry and university. His research interests are in Real Time Embedded Systems, Cyber-Physical Systems and Sensor Networks. Currently his research is includes the development of a network architecture for extreme dense sensing for active flow control. João Loureiro is a PhD candidate in Electrical and Computer Engineering in FEUP and researcher at the CISTER Research Unit.

Maia, Cláudio

PhD Student

Cláudio Maia, born in 1980, holds a degree (2007) in Computer Science Engineering at the Polytechnic Institute of Oporto.
From 2006 to 2009, he was a researcher and software engineer at Critical Software S.A. During that time, his main areas
of research were mobile and wireless communication systems and manufacturing systems.
Since October 2009, he is a Researcher in the CISTER Research Unit, involved in the CooperatES project.His main research interests are in the fields of Dynamic Distributed Real-time Systems, Operating Systems and Mobile and Wireless Communication Systems.

Marín Carrión, Ismael

PhD University of Castilla-La Mancha, Spain

Research Associate

Ismael Marín Carrión received a PhD and MRes in Advanced Computer Science from the University of Castilla-La Mancha (Spain) in 2010 and 2006 respectively, a ME in Computer Science in 2003 and a BE in Computer Systems in 2001, also from the University of Castilla-La Mancha. Ismael has held different positions in both university and industry, including several research visits. In 2013, Ismael has joined to CISTER as a postdoc researcher. The main research interests are concerned to grid computing, parallel computing and distributed systems.

Marinho, José

PhD Student

José Marinho holds an MSc degree on Electrical Engineering from the University of Coimbra (2008). He has previously worked at Instituto de Telecomunicações (Coimbra, Image Processing Lab) during his master thesis (LDPC decoding on the CELL/BE marked 20/20). Later José moved onto the Instituto de Sistemas e Robótica Coimbra (Mobile Robotics Lab) where he worked for a year period as a fresh graduate researching on and implementing bayesian inference mechanisms. José has a big interest on the embedded computing panorama. Being on the final leg of his PhD José is currently looking for opportunities to extend his knowledge in the fields of embedded operating systems and related hardware within the real-time context or other affine research fields.

Maxim, Dorin

PhD University of Lorraine, France

Research Associate

Dorin Maxim (born 29 October 1985 in Galati, Romania) received his Ph.D. degree in computer science in 2013 from the university of Lorraine, France after a three years period (2010-2013) working in the INRIA - Nancy Grand Est laboratory as part of TRIO team, under the supervision of Liliana Cucu-Grosjean and Francoise Simonot. He obtained a masters degree in computer sciences (on the topic of artificial intelligence) in 2010 and a double bachelor's degree in mathematics and theoretical computer sciences in 2008, both from the Lower Danube University in Galati, Romania. His research interests lie in the area of Real-Time Systems with particular attention to Probabilistic Analysis of Real-Time Systems.

Mekki, Maher

Undergrad Student

Maher was born in 1988 in Tunisia and he is a third year engineering student in the high school of communication Tunis (Sup'com). Currently, Maher is a trainee at Cister-Research Unit within his graduation internship. His interests are in telecommunication engineering, computer network and programming.

Moreira, Daniel

Undergrad Student

Daniel Moreira was born in 1987. Received a degree in Electrical and Computer Engineering (2010) from the Polytechnic Institute of Porto - School of Engineering. He is currently completing his MSc in Telecommunications and has been collaborating with CISTER in the field of Wireless Sensor Networks with an emphasis in mobility management and handoff mechanisms to complete his thesis on this subject.

Moreno, Maria

PhD Intern

Maria Ángeles Serna received her BSc degree in Computer Science in 2008 and her M.Sc. degree in Advanced Computer Technologies in 2010, both from the University of Castilla-La Mancha. She is also a PhD student and her research interests include collaborative processing of environmental information in wireless sensor networks, including data dissemination techniques, phenomena monitoring, modeling and simulation.

Nélis, Vincent

PhD Université Libre de Bruxelles, Belgium

Research Associate

Vincent Nélis was born in Brussels, Belgium, in 1984. In 2006 he received his master's degree in Computer Science at U.L.B. (Université Libre de Bruxelles), Belgium. During the same year, his Master's Thesis was awarded by a prestigious belgian prize: "Solvay Awards 2006". From 2006 to 2010, Vincent worked in two successful departments of U.L.B.: the "Scheduling Group" and the BEAMS (Bio-, Electro- And Mechanical Systems). In 2010, he earned his Ph.D. degree in Computer Science at U.L.B under the supervision of Prof. Joël Goossens. He is currently working at CISTER/IPP-HURRAY as a research scientist in the area of real-time scheduling theory. His research interests include: cyber-physical systems, real-time scheduling, real-time communication.

Nelissen, Geoffrey

PhD Université Libre de Bruxelles

Research Associate

Geoffrey Nelissen was born in Brussels, Belgium in 1985. He earned his MSc degree in Electrical Engineering at Université Libre de Bruxelles (ULB), Belgium in 2008. Then, he worked during four years as a PhD student in the PARTS research unit of ULB. In 2012, he received his PhD degree under the supervision of Professors Joël Goossens and Dragomir Milojevic, on the topic "Efficient Optimal Multiprocessor Scheduling Algorithms for Real-Time Systems". He is currently working at CISTER as a researcher scientist in the area of multiprocessor real-time scheduling theory. His research interests include real-time scheduling theory, real-time operating systems and multi-processors/multi-cores architectures.

Nikolic, Borislav

PhD Student

Borislav graduated at the Faculty of Electrical Engineering in Belgrade with major in Computer Science in 2007. He spent almost two years in industry developing large-scale enterprise applications. Currently, Borislav is doing his PhD at CISTER/IPP-HURRAY Research unit. He is amateur road cyclist and big fan of FC Red Star Belgrade. His research interests include real time and embedded systems, distributed and parallel computing, gossip protocols, ORMs and software architecture and design.

Noda, Claro

PhD Student

Claro Noda graduated in Physics from University of Havana, Cuba in 1996. He worked in Scientific Instrumentation at the Superconductivity Laboratory, IMRE (1996-2001) where he completed his Master in Physical Sciences in 2000 and later continued research activities at the "Henri Poincaré" Complex Systems Group. He has also taught at the General Physics Department in the Faculty of Physics in Havana (2005-2008). Currently he's a MAP-Tele PhD student at University of Minho and a researcher at CISTER/ISEP, Portugal.

Nogueira, Luis Miguel

PhD University of Porto, Portugal

Professor, Research Associate

Luís Nogueira got his BSc in Computer Engenineering at the School of Engineering, Polytechnic Institute of Porto, in 2000. In 2002, got his MSc and in 2009 his PhD in Informatics (Systems and Networks) at the Faculty of Science, Univeristy of Porto. Since 2001 he is teaching assistant at the Department of Computer Engineering of the School of Engineering of the Polytechnic Institute of Porto. From 2000 to 2003 he was a researcher at NIAD&R (Distributed Artificial Intelligence & Robotics Group) of LIACC (Artificial Intelligence and Computer Science Lab), University of Porto. Now, his current research interests are in the fields of Dynamic Distributed Real-time Systems, Quality of Service and Ad-hoc Networks.

Pacheco, Filipe

PhD University of Porto, Portugal

Research Center Adjunct Director

Professor, Research Associate

Filipe de Faria Pacheco Paulo (born Filipe de Faria Pacheco in 1971) has a degree (1994), MSc (1997) and PhD (2009) in Electrical and Computer Engineering at the University of Porto. Since 1996 he is a teaching assistant at the Department of Computer Engineering, - School of Engineering of the Polytechnic Institute of Porto. He was researcher at the Systems and Robotics Institute, Industrial Automation Group (University of Porto), from 1994 to 1996, in the area of User Interfaces. He is currently working in Multimedia and Real-Time networks projects.

Pacheco, João

Undergrad Student

João Pacheco was born on 1994 in Porto. He is enrolled in the bachelors in Computer Engineering at Instituto Superior de Engenharia do Porto.

Pasdeloup, Bastien

Undergrad Student

Bastien Pasdeloup was born in 1988 in Brest, France. He started his studies in computer science in 2008 when he entered an Associate Degree in Brest. After a year at ENIB, a French engineering school, he decided to dedicate himself to research, and applied to ENS Cachan, Brittany extension, where he is still studying.
His interests are very varied, and cover many fields of computer science, from system to high level programming languages, also including fields such as security and machine learning.
He will stay in Porto for his internship from the 20th of May to the end of August.

Pedro, André

PhD Student

André Pedro was born in Covilhã, Portugal, in 1987. In 2009 he received his degree in Computer science engineering at Universidade da Beira Interior, Covilhã. In 2011 he has concluded the Master's degree in Computer science engineering at Universidade do Minho, Braga with thesis "Learning and testing Stochastic discrete event systems". Now, he begin his Phd study where must be highlighted the Ada contracts for verification of real-time systems. His research interests include: discrete event systems, real-time scheduling, and model-checking.

Pereira, David

PhD MAPi, Portugal

Research Associate

David Pereira was born in Porto, Portugal, in 1980. In 2003 he received his degree in Computer Science at University of Porto. In 2007 he finished his Master's degree in Computer Science also in University of Porto, in the areas of formal logics for specifying and reasoning about intelligent agents. He has a PhD in Computer Science, in the MAP-i PhD program, organized by the Universities of Minho, of Porto and of Aveiro. His research is focused in the mechanization of Kleene algebra and Kleene algebra with tests in the Coq theorem prover (see http://coq.inria.fr/). He also mechanized a deductive proof system for dealing with the partial correctness of parallel programs, under the spirit of Rely/Guarantee thinking. Besides being a happy Coq user and adept of formal program verification, David is keen to apply is formal methods background into the realm of programming languages for real-time programs, namely the well-know and powerful Ada.

Pereira, Miguel

Technical Staff

Nuno Miguel Pereira was born in 1972 at Lisbon, worked from 1996 to 1998 at Efacec in manufacture of Power transformers. Since then he turned to computers and audiovisual equipment at end-user market, business market and educational market.
His interests are home cinema, new technologies and renewable energies.

Pereira, Nuno

PhD University of Minho, Portugal

Professor, Research Associate

Nuno Pereira received a degree in computer engineering from the School of Engineering, Polytechnic Institute of Porto, Porto, Portugal, a M.Sc. and Ph.D. degrees from the University of Minho, Braga, Portugal, in 2002 and 2005 and 2010 respectively. He is a researcher at CISTER, a top-ranked research unit of the Portuguese research system since 2001. He started his research work dedicated to traffic scheduling combining multimedia and industrial communication protocols, and also analyzed the timing behavior of several industrial communication protocols. More recently, Nuno developed novel medium access control protocols for wireless networks and explored efficient ways to obtain aggregated quantities in large scale, dense wireless networks.

Petters, Stefan M.

PhD Technical University Munich, Germany

Research Centre Vice-Director

Research Associate

My research interests include real time and embedded systems in general and more specifically system energy management, mixed-criticality systems, adaptive real-time systems, (probabilistic) worst case execution time (WCET) analysis, and (probabilistic) schedulability analysis.

Pinho, Luis Miguel

PhD University of Porto, Portugal

Research Centre Vice-Director

Professor, Research Associate

Luis Miguel Pinho has a MSc (1997) and a PhD (2001) in Electrical and Computer Engineering at the University of Porto. He is Coordinator Professor at the Department of Computer Engineering - School of Engineering of the Polytechnic Institute of Porto, and Vice-Director and Research Associate at the CISTER research unit, where he currently leads the real-time software research line. His main research interest is on the software infrastructure for real-time embedded systems, in particular languages and operating systems. He is especially interested in Ada, the best language for real-time embedded systems. Miguel is a member of ISO/IEC JTC1/SC22/WG9 and board member of Ada-Europe. He served as General Chair and Program Co-Chair of the Ada-Europe 2006 conference, was a Keynote Speaker at RTCSA 2010 and Program Co-Chair of Ada-Europe 2012. He is Editor-in-Chief of the Ada User Journal, and a member of the HiPEAC network of excellence.

R., Raghu

PhD IIT Bombay, India

Research Associate

Raghu received his PhD from IIT Bombay in 2009. He was at Motorola Labs Bangalore, since 2008, working on protocol analysis in data wireless networks. After leaving the labs, he started a firm consulting in wireless systems design and development. He is currently at CISTER, ISEP, Porto. His areas of interest include architecting and building sensor network systems and especially, developing low cost solutions using open standards and COTS.

Raravi, Gurulingesh

PhD Student

Gurulingesh Raravi finished his Masters Degree at IIT Bombay in 2005. He has three years of working experience. Currently, he is pursuing PhD in the area of Real-Time Scheduling on Heterogeneous Multiprocessor Platform.

Ribeiro, André

IT Support

André Ribeiro was born in 1991 in S. João da Madeira. In 2009, André finished his high school degree specialised in Information System's Management and Programming, and in 2012 his Bachelor in Informatics Engineering/Computer Science. Currently, André is enrolled at ISEP, in the Master Programme in Informatics Engineering/Computer Science.

Robles, Ramiro

PhD University of Leeds, UK

Research Associate

Ramiro Sámano Robles obtained his degree in Telecommunications engineering from the national university of Mexico in 2001. He has professional experience ad PCB design engineer for high frequency applications and for the design of radio-frequency up-converters for 2.1 GHz communications. He has also professional experience as new technology evaluation engineer for a major cellular operator in Mexico where he was responsible for one of the first trials for 2.5G and 3G CDMA200 networks in Latin-america, and the implementation of several other new technologies such as intelligent network, smart antennas, localization-based services and short message services.

He obtained the PhD in signal processing for wireless communications from the University of Leeds in 2007, and MSc in Telecommunications and Information Systems from the University of Essex in 2003. He held a postdoctoral position at the Institute of Telecommunications in Aveiro, Portugal, where he was involved in the management and scientific contribution of several FCT and FP7 European research projects related to distributed MIMO, RFID, Internet of things (IOT), radio-over-fibre distributed antenna systems, cooperative systems, and cognitive radio. Some of these projects were FUTON (www.ict-futon.eu), CODIV(www.ict-codiv.eu), ASPIRE (www.fp7-aspire.eu) and QoSMOS (www.ict-qosmos.eu). His area of contribution in these projects was mainly in the interactions and optimization of MAC, PHY and RRM (Radio resource management) layers, particularly for their integration in system level simulators and testbeds for LTE, EPC and WiMAX standards..

Rodrigues, Marco

Undergrad Student

Marco Rodrigues was born in 1994 in Porto. Is in the second year of the degree in computer engineering at ISEP. Its main interest is programming. Is committed to improving their skills, and learn more about the software-hardware interaction.

In his spare time, enjoys playing the piano and find out more about the technologies that surround us.

Sanchez, Francisco

PhD Student

Francisco Sánchez was born on 1985 in Santo Domingo, Dominican Republic. He received his Bachelor's Degree in Electronics and Communications Engineering from the Instituto Tecnológico de Santo Domingo (INTEC) in 2009 and M.Sc. Degree on Information and Communication Technology from Technical University of Cartagena in 2010.
Currently, Francisco is pursuing a PhD in Information and Communication Technology at the Technical University of Cartagena. His main research interests are: Model Driven Engineering (MDE), Software Design Patterns and Real Time Systems.

Sandim, Miguel

Undergrad Student

Miguel Sandim is an undergraduate student at the Faculty of Engineering of the University of Oporto taking a degree in Informatics and Computing Engineering. His main interests include hardware programming, algorithm design and mathematics.

Santos, Pedro

Technical Staff

Pedro Santos was born in 1994 in Porto, and is currently enrolled in the 2nd year of the FEUP's course, in Electrical and Computer Engineering, at the University of Porto. His main interests are in the fields of Wireless Sensor Networks, Real-time Systems, Programming, Artificial Intelligence, Automation and Electronics Systems.

Severino, Ricardo

Lecturer, PhD Student

Ricardo Severino was born in 1982 and has a Degree (2006), and a MSc (2008) in Electrical and Computer Engineering at the Polytechnic Institute of Porto – School of Engineering (ISEP/IPP). Since 2006, he has been working in the area of Wireless Sensor Networks, namely on improving quality-of-service (QoS) in WSNs by using standard and commercial-off-the-shelf (COTS) technology, at CISTER. In this line, he has been actively participating in the ART-WiSe and Open-ZB research frameworks, as well as in international projects such as ArtistDesign, CONET, and EMMON. He is also a founding member and contributor of the 15.4 and ZigBee TinyOS Working Groups. Recently, his MSc Thesis work was awarded with the EWSN'09 Best MSc Thesis Award at the prestigious European Conference on Wireless Sensor Networks (EWSN'09).

Silva, Eduardo

Technical Staff

Eduardo Silva was born in 1975 at Porto, Portugal, from 1994 to 1998 he attended Advertising at Universidade Fernando Pessoa, from 1999 to 2013 worked as computer technician in the final-costumer market.
His main interests are Information Technologies and Astronomy.
He dreams that one day he may have a quantum computer at his desk.

Soares, Bruno

Undergrad Student

Bruno Soares, born in 1989, is a third-year student in Computer Engineering at the School of Engineering of the Polytechnic Institute of Porto. He's currently working on a code mobility library for Android operating systems. His main interests are mobile programming, software engineering, and networks.

Sotomaior, Tomás

Undergrad Student

Tomás Sotomaior was born in 1990 in S. Mamdede Infesta. In 2008, Tomás finished his High School Technological Course in informatics. Currently, he is enrolled in the 3rd year of the ISEP's course in Computer Engineering at the School of Engineering, Polytechnic Institute of Oporto, and is doing is internship at CISTER Research Group, working on distributed parallel programming techniques.

Sousa, Paulo Gandra de

PhD University of Minho, Portugal

Professor, Research Associate

Paulo Gandra de Sousa is a Professor of Informatics at Instituto Politécnico do Porto (Polytechnic Institute of Porto, Portugal) - ISEP/IPP since 1996. He graduated in 1995 from ISEP-IPP; in 1998, he concluded a post-graduation on "Distributed Systems, Computer Architectures and Computer Communications" at Universidade do Minho (University of Minho, Portugal), and achieved his PhD in 2002 (also from Universidade do Minho). He worked for 3 years as an application developer for a Portuguese software house in the field of electronic archive, database retrievals and component development. Prior to CISTER he was a member of the R&D Group on Knowledge Engineering and Decision Support (GECAD, ISEP/IPP) and the technical contact point for the ISEP/IPP node of AgentLink – European Network of Excellence in Agent Based computing. He is one of the founders of the Portuguese chapter of the International Association of Software Architects (IASA). His main research interests are Distributed (Intelligent) Systems, Large Scale Systems, and Enterprise Application Architectures.

Sousa, Paulo Baltarejo

PhD University of Porto, Portugal

Lecturer, Research Associate

Paulo Baltarejo Sousa received a degree in computer engineering from the School of Engineering, Polytechnic Institute of Porto, in 2003. In 2007, he received an MSc in Electrical and Computer Engineering from Technical Institute, Technical University of Lisbon. In 2013, he received a PhD in Informatics Engineering from Faculty of Engineering, University of Porto. Since 2003 he is teaching assistant at the Department of Computer Engineering of the School of Engineering of the Polytechnic Institute of Porto and also research at CISTER. Now, his current research interests are in the field of real-time scheduling algorithms for multiprocessor systems with special focus on implementations in operating systems.

Souto, Pedro

PhD Stony Brook University, USA

Professor, Research Associate

Pedro Ferreira do Souto, received a Licenciatura in Electrical Engineering from the University of Porto in 1986, and a Ph.D. in Computer Science from the Stony Brook University, USA, in 1999. He is a Assistant Professor at the Department of Informatics Engineering of the Faculty of Engineering of the University of Porto.

His research interests include distributed systems, fault-tolerance, real-time systems and multiprocessing.

Teixeira, José

Undergrad Student

José was born in 1991 in Porto. José has a high school degree specialized in Information System's Management and Programming. Currently, he is enrolled in the 3rd year of the ISEP's course in Computer Engineering at the School of Engineering, Polytechnic Institute of Oporto, and is doing is internship at CISTER Research Group, working on code offloading for mobile systems.

Teixeira, César

MSc Student

César Teixeira, born in 1987, holds a degree (2010) in Computer Science Engenineering at the School of Engineering, Polytechnic Institute of Oporto. Currently he is involded in the ENCOURAGE project.His main interests are in the field of Networking, Mobile, Multi-Agent Systems and Web development.

Thamri, Meriam

Undergrad Student

Meriam Thamri was born in 1988 in Tunisia. Currently, she is a third year engineering student at the Higher School of Communication of Tunis (Sup'Com). For her graduation project, she was accepted as a trainee for a 6 month internship in the CISTER Research Unit. Her work will be focused on wireless sensor networks and the handoff process. Her interests are mainly in the areas of information and communication technologies, mathematics and programming.

Tovar, Eduardo

PhD University of Porto, Portugal

Research Centre Director

Professor, Research Associate

Eduardo Tovar is the head of CISTER Research Center. He was born in 1967 and has received the Licentiate, MSc and PhD degrees in electrical and computer engineering from the University of Porto, Porto, Portugal, in 1990, 1995 and 1999, respectively. Currently he his Professor of Industrial Computer Engineering in the Computer Engineering Department at the Polytechnic Institute of Porto (ISEP-IPP), where he is also engaged in research on real-time distributed systems, wireless sensor networks, multiprocessor systems, cyber-physical systems and industrial communication systems. He heads the CISTER Research Center, a top ranked ("Excellent") unit of the FCT Portuguese network of research units. Since 1991 he authored or co-authored more than 100 scientific and technical papers in the area of real-time computing systems, wireless sensor networks, distributed embedded systems and industrial computer engineering. Eduardo Tovar has been consistently participating in top-rated scientific events as member of the Program Committee, as Program Chair or as General Chair. Examples are: IEEE RTSS (Real Time Systems Symposium); IEEE RTAS (Real-Time and Embedded Technology and Applications Symposium); IEEE SDRS (Symposium on Distributed Reliable Systems); IEEE ICDCS (International Conference on Distributed Computing Systems); ACM EMSOFT (Annual ACM Conference on Embedded Software); Euromicro ECRTS (Euromicro Conference on Real-Time Systems); IEEE ETFA (Emerging Technologies on Factory Automation) or IEEE WFCS (Workshop on Factory Communication Systems). He is team leader within the 6th Framework IST Network of Excellence ARTIST2, on distributed embedded systems.

Ullah, Sana

PhD Inha University, South Corea

Reseach Associate

Sana Ullah received his Ph.D. degree in Information and Communication Engineering from Inha University in 2011. He worked as an assistant professor in the College of Computer and Information Science, King Saud University, Riyadh from Dec. 2011 to Mar. 2014. He currently serves as an editor for Springer Journal of Medical Systems, KSII Transaction of Internet and Information Systems (TIIS), Wiley Security and Communication Network (SCN), Journal of Internet Technology and International Journal of Autonomous and Adaptive Communications Systems (IJAACS). He served as a guest editor for many top journals including Elsevier Journal of Information Science (INS), Springer Journal of Medical System (JOMS), and Springer Journal of Telecommunication Systems (TS). He also served as a co-chair/TPC member for a number of international conferences including BodyNets, IEEE PIMRC, IEEE Healthcom, IEEE Globecom, and IEEE WCNC.

He is currently working as a Research Scientist at CISTER Research Unit at ISEP/IPP.

Vahabi, Maryam

PhD Student

Maryam Vahabi received her degree in Electrical Engineering from University of Guilan in 2003. She obtained her Master of Science in Communication Network Engineering from University Putra Malaysia in 2009 and her Master research was on wireless sensor networks. She has joined the IPP-HURRAY! in July, 2009. Currently, she is doing her PhD in CISTER/IPP-HURRAY Research unit. Her current research interests are sensor networks, real-time systems and schedulability analysis.

Vergueira, Marco

Undergrad Student

Marco Vergueira was born in 1988 in Valpaços, Portugal. From an early age acquired a passion for engineering. Currently, he is enrolled in the 3rd year of the ISEP's course in Computer Engineering at the School of Engineering, Polytechnic Institute of Oporto, and is doing is internship at CISTER Research Group, his main research interests are in embedded systems and high level software

Yomsi, Patrick Meumeu

PhD Université Paris Sud, France

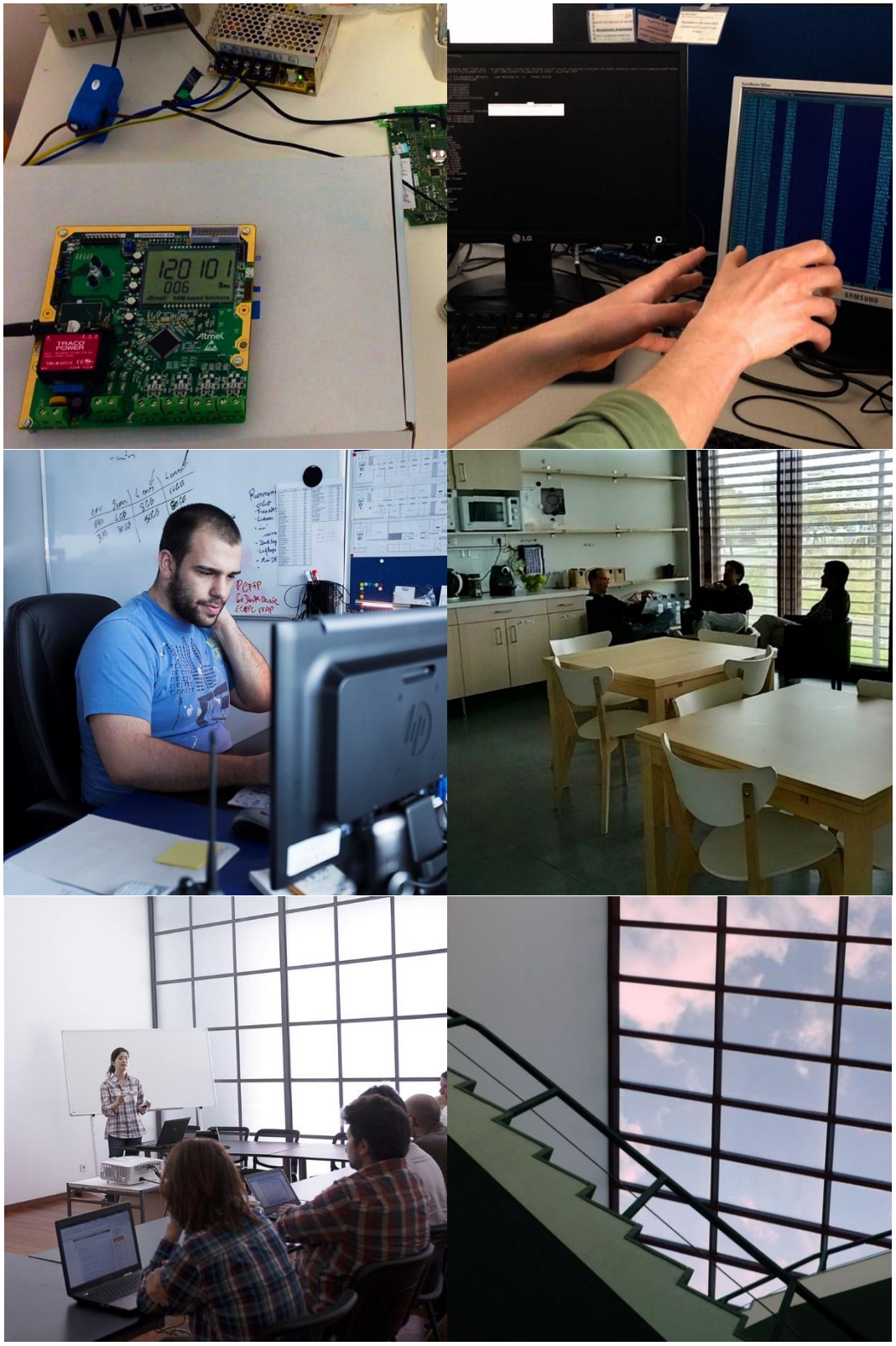
Research Associate

Patrick Meumeu Yomsi received his Ph.D. degree in 2009 from the Université Paris Sud, Orsay in France. After his degree, he worked in a number of research projects addressing various aspects of real-time computing systems. He was successively a member of AOSTE Research Unit at the French National Institute in Computer Science and Control (INRIA) in Paris Rocquencourt, France, then a member of PARTS Research Unit at Université Libre de Bruxelles (ULB) in Brussels, Belgium, and finally a member of TRIO Research Unit at INRIA in Nancy, France. He is currently a Research Scientist at CISTER Research Unit at ISEP/IPP. His research interests include real-time scheduling theory, real-time communication and real-time operating systems.

Facilities

www.cister.isep.ipp.pt/info

CISTER has evolved gradually (in the last 15 years) from a few rooms at ISEP Campus to an entirely new building. This single-home (2000 m2 area) is a strong asset which will help the unit to continue to meet the demands and challenges of the current and future projects and to pursue high-standard work plan that matches the best in the world in the area of RTES.



CISTER
Research Center in
Real-Time & Embedded
Computing Systems

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