CISTER
Research Center in
Real-Time & Embedded
Computing Systems

Annual Report

2013

isep Instituto Superior de Engenharia do Porto

POLITÉCNICO DO PORTO

INESCTEC
TECNOLOGIA E CIÊNCIA

Contents

Executive Summary

www.cister.isep.ipp.pt

The Research Centre in Real-Time and Embedded Computing Systems (CISTER) is based upon a research group created in 1997 at the School of Engineering (ISEP) of the Polytechnic Institute of Porto (IPP). Since then it has grown to become the most prominent research unit of IPP and one of the leading international research centres in real-time and embedded computing systems. In both the 2003 and 2007 evaluation processes, the Unit was granted the classification of 'Excellent' (the highest possible mark at that time) from an international panel of experts, being the only Portuguese unit in the areas of Electrical Engineering and Computer Science and Engineering to top-rank in both evaluations.

The strategy laid out by the Unit has been from the start towards top-quality research, able to compete with the best international groups in our research areas.

CISTER focuses its activity in the analysis, design and implementation of Real-Time and Embedded Computing Systems (RTES).

The goal of the unit is to continue (and reinforce) to be one the International leaders of research in real-time embedded systems. This objective is aligned with the growing strategic importance of embedded systems in Europe, and the role that needs to be played in the international research landscape of the area.

CISTER is hosted by ISEP, the main management institution. CISTER and ISEP have recently entered (since 2011) a strategic alliance with the INESC-TEC Associated Laboratory in which CISTER became an autonomous unit of INESC-TEC. It is our belief that this allows the continuation of the synergies in a challenging future environment.

Management Structure

The research unit is led by a Board of Directors, a Scientific Board and an External Advisory Board. The Board of Directors, is led by the unit's Director/ Coordinator, and includes Vice Directors and an Adjunct Director. The main responsibilities of the Director are: to represent the Unit externally; to manage and co-ordinate the activities of the Unit; to co-ordinate the definition of the plan of activities and budget. The Scientific Board, which includes all the members of the Unit with a PhD degree, has the following main responsibilities: to appoint the Director; to define the scientific research areas and working strategies; to carry out research; and to approve the plan of activities, budget and yearly report.

Board of Directors: Eduardo Tovar (Director), Luis Miguel Pinho (Vice-Director) Stefan M. Petters (Vice-Director), Filipe Pacheco (Adjunct-Director).

The activities of the unit are periodically reviewed by the External Advisory Board. Annually, interactions (including on-site visits) are devised to discuss activities, exploitation of results and future plans of the unit.

External Advisory Board: Tarek Abdelzaher, University of Illinois at Urbana-Champaign, USA; Sanjoy Baruah, University of North Carolina at Chapel Hill, USA; Alan Burns, The University of York, United Kingdom; Rodrigo Maia, Critical Software, Portugal; Daniel Mossé, University of Pittsburgh, USA; Michael Paulitsch, EADS, Germany; Sérgio Penna, Embraer, Brazil; Zlatko Petrov, Honeywell, Czech Republic; Raj Rajkumar, Carnegie-Mellon University, USA.

CISTER in Numbers

CISTER is currently housed in an entirely new building exclusively devoted to its R&D activities. This single-home (2000 m2) is a strong asset to continue to compete among the best in the world in the area of RTES.

CISTER has a strong and solid international reputation, built upon a robust track record of publications (80 publications in 2013), a continuous presence on program and organizing committees of international top conferences. In 2013 CISTER has over 60 collaborators, covering more than 20 nationalities. Around one third of the researchers have PhD.

The unit had a 2013 budget around 870K EUR of competitive funding. During 2013 we had 7 international and industrial driven projects running, and 11 fundamental research projects (FCT supported).

In 2013, CISTER also got approved a set of new projects that accounts for a budget 700K EUR, while the total budget of projects initiated totals 1333K EUR.

Focus and Research Lines

www.cister.isep.ipp.pt/research

CISTER focuses its activity in the analysis, design and implementation of Real-Time and Embedded Computing Systems (RTES). In these systems, correctness depends not only on the logical result of computation, but also on the time at which the results are produced. This implies that, unlike more traditional information and communication systems, where there is a separation between correctness and performance, in real-time systems correctness and performance are very tightly interrelated. Furthermore, considering their tight integration with the surrounding environment, RTES require a more holistic and integrated system perspective. Historically, RTES were an important, but narrow, niche of computer systems, consisting mainly of military systems, air traffic control and embedded systems for manufacturing and process control. Meanwhile, both the emergence of large-scale distributed systems and the pervasiveness of embedded devices, enabled by advances in technology, has broaden real-time concerns into a mainstream enterprise, with clients in a wide variety of industries and academic disciplines. This trend has established real-time embedded systems technology as a priority for commercial strategy and academic research for the foreseeable future and also for a wider number of applications.

Real-Time Embedded Systems technologies are deployed in almost all relevant market sectors across Europe. Consequently, Embedded Systems have a major impact on the way these sectors work and collaborate, how they will develop, how they are perceived by both professionals and the public, and how successful their products will be on the world market. Real-Time Embedded Computing Systems is one of the strategic research and innovation areas in Europe, with impact in very important sectors such as industrial automation, automotive, aerospace, consumer electronics, communication systems and medical systems. For many of these sectors, Europe is a world-wide reference, contrary to general-purpose computing systems, traditionally dominated by non-European organizations.

Wireless Sensor Networks (WSN)

Wireless Sensor Networks (WSNs) are triggering a new era in Information and Communication Technologies. These networks of tiny embedded computing systems are enabling a new set of large-scale monitoring and control applications such as for pervasive Internet, homeland security, critical physical infrastructures monitoring, precision agriculture, environmental monitoring or intelligent transportation systems.

CISTER has been assuming international leadership in the WSNs scientific area, namely on supporting Quality-of-Service (QoS), particularly focusing on timeliness and real-time, reliability and energy-efficiency aspects.

We are addressing the use of both standard and COTS technology and cutting-edge solutions designed from scratch. CISTER pursues excellence-level collaborative R&D sustained by analytical, simulation and experimental models. We have recently designed, implemented and deployed the largest WSN test-bed in Europe to date, with 300+ sensor nodes.

Multicore Systems

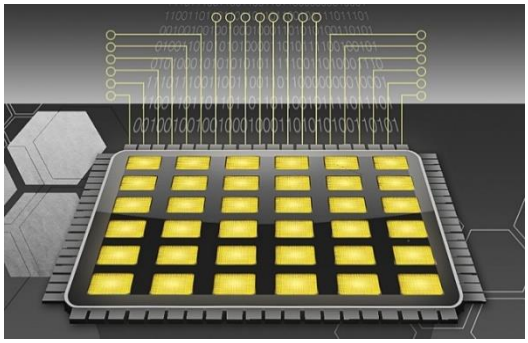


Illustration: Christine Daniloff/MIT

Multicores are spreading at an unprecedented rate. Today, a multicore processor is the default choice in server/desktop/laptop computers and

it is increasingly used in embedded computer systems (such as celular phones, in-vehicle electronics and medical instrumentation).

The use of multicores in embedded systems is complicated by the fact that many embedded computer systems have real-time requirements, that is, the time at which a program produces its result is as important as the result itself. The time at which a program computes its result depends on how computer resources (processor cores, memory, bus bandwidth, I/O devices, etc.) are shared among programs and therefore the scientific community has created a toolkit of algorithms for scheduling programs on a single processor so that the program executes at the right time. Unfortunately, scheduling programs at the right time on a multicore is currently not well understood; in particular, there is no such well-established toolkit for multiprocessors.

Researchers at CISTER/IPP-HURRAY are currently developing scheduling algorithms and proof techniques which makes it possible to prove at design time that deadlines will be met at run-time, even if the exact time when programs request to execute is unknown.

Cyber-Physical Systems (CPSs)

Although the IT transformation in the 20th century appeared revolutionary, a bigger change is probably yet to come. The terms "Cooperating-Objects" or "Cyber-Physical Systems (CPS)" have come to describe the research and technological effort that will ultimately efficiently allow interlinking the real world physical objects and cyberspace. Actually the integration of physical processes and computing is not new. Embedded systems have been in place since a long time to denote systems that combine physical processes with computing. The revolution will come from extensively networking embedded computing devices, in a blend that involves sensing, actuation, computation, networking, pervasiveness and physical processes.
Such extreme networking poses considerable technical challenges

ranging from the (distributed) programming paradigms (languages still lacking temporal semantics, suitable concurrency models and hardware abstractions) to networking protocols with timeliness as a structuring concern, and including systems theory that combines "physical concerns" (control systems, signal processing, etc.) and "computational concerns" (complexity, schedulability, computability, etc.).

Synapticon SOMANET

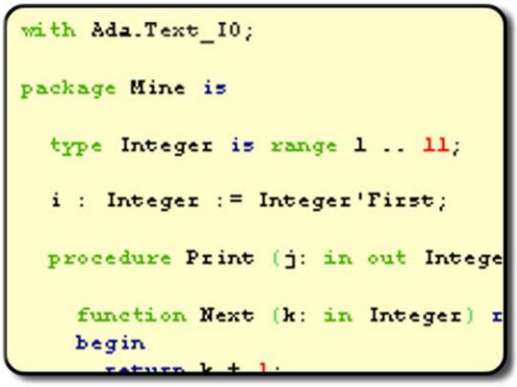
Adaptive Real-Time Systems

ADEX

We are increasingly surrounded by computer controlled devices. Many of which are not perceived as "computers" and are called embedded systems: think of mobile phones, cars, or aircraft. Many of these systems have some sort of real-time requirements, be it responsiveness, quality of service or hard deadlines, where the miss of the latter leads to catastrophic consequences. Beyond the fact that we are more and more surrounded and dependent on such systems, there is another trend visible. Embedded systems are often networked and/or receive upgrades and extensions during the lifetime of an individual system. These may be, for example, applications downloaded to your mobile phone or an upgrade of your motor control in a garage. A third trend is an increase in mobile systems, requiring effective power management to extend the battery lifetime.

Within this research line we address the issues associated with systems requiring temporal isolation of system parts with different criticality, as well as systems being robust and reliable in the context of additional restrictions like available energy, changing environment or a dynamic set of tasks executed on such a system.

Real-Time Software



The current use of software as the key component of any real-time embedded system is increasing the, often contradictory, demands for attributes such as flexibility, adaptation, isolation, reliability or availability. Software infrastructure (such as languages, operating systems, middleware) and models are, more and more, a fundamental topic for system development, being transversal to application areas and research domains.

In this context, this research line addresses issues associated with the software infrastructure required for developing embedded real-time systems. Our approach is to integrate advanced mechanisms within programming languages, operating systems and middleware, allowing designers and programmers to manage the increasing complexity, and flexibility requirements, simultaneously reducing common errors, and allowing isolation and verification of systems.

Research Projects

www.cister.isep.ipp.pt/projects

International & Industrial Driven Projects

Arrowhead

Ahead of the future

JU grant nr. 332987 ARTEMIS/0001/2012
Funding: 67.6MEUR (CISTER Funding: 207KEUR)

4 years (Mar 2013 to Feb 2017)

Our society is facing both energy and competitiveness challenges. These challenges are tightly linked and require new dynamic interactions between energy producers and energy consumers, between machines, between systems, between people and systems, etc. Cooperative automation is the key for these dynamic interactions and is enabled by the technology developed around the Internet of Things and Service Oriented Architectures.

The objective of the Arrowhead project is to address the technical and applicative challenges associated to cooperative automation: provide a technical framework adapted in terms of functions and performances; propose solutions for integration with legacy systems; implement and evaluate the cooperative automation through real experimentations in applicative domains: electro-mobility, smart buildings, infrastructures and smart cities, industrial production, energy production and energy virtual market; point out the accessible innovations thanks to new services; lead the way to further standardization work.

The strategy adopted in the project has four major dimensions: an innovation strategy based on business and technology gap analysis paired with a market implementation strategy based on end users priorities and long term technology strategies; application pilots where technology demonstrations in real working environments will be made; a technology framework enabling collaborative automation and closing innovation critical technology gaps; an innovation coordination methodology for complex innovation "orchestration"

Partners of the Arrowhead consortium include, among others:

CarCoDe

Platform for Smart Car to Car Content Delivery

ITEA2 N° 11037, QREN N° 30345
Funding: 399KEUR (CISTER Funding: 58KEUR)

2 years (Jul 2013 to Jun 2015)

CarCoDe will develop a software platform which enables traffic service ICT ecosystems and business opportunities to be evoked. The objective is to offer a merging layer between automotive industry, traffic service operators, and third party developers. CarCoDe is an ITEA2 labeled European project. Portuguese partners are funded in the scope of a national QREN project.

Partners of the CarCoDe consortium include, among others:

CONCERTO

Guaranteed Component Assembly with Round Trip Analysis for Energy Efficient High-integrity Multi-core Systems

JU grant nr. 333053 ARTEMIS/0003/2012
Funding: 9.56MEUR (CISTER Funding: 375KEUR)

3 years (May 2013 to Apr 2016)

Emerging embedded systems platforms harnessing new heterogeneous, multicore architectures to enable the next generation of powerful mission-critical applications are demanding across-the-board advances in all areas of design and development to fulfil their promise. The integration of component-based design with model-driven development creates a potent combination especially capable of mastering the complexity of these new systems. CONCERTO will deliver a reference multi-domain architectural framework for complex, highly concurrent, and multi-core systems, where non-functional properties (including real-time, dependability, and energy management) will be established for individual components, derived for the overall system at design time, and preserved by construction and monitoring at run-time.

The CONCERTO framework that will be developed in the project will integrate: Correctness-by-construction for multicore systems with innovative model-to-code transformation techniques targeted at their special characteristics. A multi-view, hierarchical cross-domain design space sufficiently rich to enable a compositional approach to the next generation of complex, heterogeneous platform architectures. Support for iterative and incremental development of multicore systems through simulation and early model-based analysis, with fully automated back propagation of

results to the user model. Hardware modelling facilities equipped to cope with the new generation of heterogeneous, multicore platforms. Advances in run-time monitoring of mission- and operation-critical non-functional properties such as energy consumption on partitioned and multicore processor architectures. The applicability of the CONCERTO solutions to multiple industrial domains (including aerospace, telecoms, automotive, petroleum and medical) will be ensured through the elaboration of representative industrial use cases.

CONCERTO builds on the previous CHESS project results from the ARTEMIS programme, as well as the results of several other related projects.

Partners of the CONCERTO consortium include, among others:

HiPEAC 3

European Network of Excellence on High Performance and Embedded Architecture and Compilation

FP7-ICT-287759
Funding: 3.8 MEUR

3 years (Jan 2013 to Dec 2015)

As part of the research coordination program, HiPEAC3 includes a new instrument, called Thematic Sessions. A Thematic Session is a natural evolution of the clusters and task forces in HiPEAC2, but more reactive and self-organized. In HiPEAC3, any partner or member can propose a thematic session, on condition that it is related to the HiPEAC vision. A thematic session is comparable to an informal workshop. Proposers of a thematic session are encouraged to involve the FP7 projects and HiPEAC companies in the session they propose. In that sense a thematic session is very similar to the organization of a cluster meeting in HiPEAC2. Collaboration and networking between member institutions and across the different disciplines: computer architects, design tool builders, compiler builders, system designers, between researchers from academia and industry, between European and non-European institutions. This collaboration between best of breed must lead to more European excellence in the HiPEAC domain. Collaboration and networking is stimulated by various networking events, and the small collaboration incentives like collaboration grants, mini-sabbaticals, internships.

Valorisation of research results in the form of highly visible publications and commercialization of research results by existing companies or by newly created companies. The goal is to help companies to achieve world-leading positions in the computing systems and computing products, and to further increase Europe's worldwide visibility in the domain via the HiPEAC conference, the ACACES summer school, the HiPEAC journal, a newsletter, a website,

seminars, technical reports, workshops, and awards.

ENCOURAGE

Embedded iNtelligent COntrols for bUildings with Renewable generAtion and storaGE

JU grant nr. 269354 ARTEMIS/0002/2010
Funding: 6.37MEUR (CISTER Funding: 266KEUR)

42 months (Jun 2011 to Nov 2014)

The ENCOURAGE project aims to develop embedded intelligence and integration technologies that will directly optimize energy use in buildings and enable active participation in the future smart grid environment. The desired energy savings will be achieved in three complementary ways:

I. by developing supervisory control strategies that will be able to coordinate larger subsystems and orchestrate operation of the numerous devices in such systems.
II. through an intelligent gateway with embedded logic supporting inter-building energy exchange.
III. by developing novel virtual sub-metering technologies and event-based middleware applications that will support advanced monitoring and diagnostics concepts.

The primary application domains are non-residential buildings and campuses, but the project has relevancy also to residential buildings and neighbourhoods. This will be expressed through several demonstrators comprising public and private office buildings, campus buildings, and private homes. ENCOURAGE aims to achieve 20% of energy savings through the improved interoperability between various types of energy generation, consumption and storage devices; inter-building energy exchange; and systematic performance monitoring.

Partners of the ENCOURAGE consortium include, among others:

P-SOCRATES

Parallel SOftware framework for time-CRitical mAny-core sysTEmS

FP7-ICT-611016
Funding: 2.76MEUR (CISTER Funding: 544KEUR)

3 years (Oct 2013 to Sep 2016)

The recent technological advancements and market trends are causing an interesting phenomenon towards the convergence of High-Performance Computing (HPC) and Embedded Computing (EC) domains. On one side, new kinds of HPC applications are being

required by markets needing huge amounts of information to be processed within a bounded amount of time. On the other side, EC systems are increasingly concerned with providing higher performance in real-time, challenging the performance capabilities of current architectures. The advent of next-generation many-core embedded platforms has the chance of intercepting this converging need for predictable high-performance, allowing HPC and EC applications to be executed on efficient and powerful heterogeneous architectures integrating general-purpose processors with many-core computing fabrics. To this end, it is of paramount importance to develop new techniques for exploiting the massively parallel computation capabilities of such platforms in a predictable way.

P-SOCRATES will tackle this important challenge by merging leading research groups from the HPC and EC communities. The time-criticality and parallelisation challenges common to both areas will be addressed by proposing an integrated framework for executing workload-intensive applications with real-time requirements on top of next-generation commercial-off-the-shelf (COTS) platforms based on many-core accelerated architectures. The project will investigate new HPC techniques that fulfil real-time requirements.

The main sources of indeterminism will be identified, proposing efficient mapping and scheduling algorithms, along with the associated timing and schedulability analysis, to guarantee the real-time and performance requirements of the applications.

Partners of the P-SOCRATES consortium include, among others:

RECOMP

Reduced Certification Costs for Trusted Multi-core Platforms

Artemis 100202
Funding: 25.8MEUR (CISTER Funding: 456KEUR)

3 years (Apr 2010 to Mar 2013)

RECOMP recognizes the fact that the increasing processing power of embedded systems is mainly provided by increasing the number of processing cores. The increased numbers of cores is commonly regarded as a design challenge in the safety-critical area, as there are no established approaches to achieve certification. At the same time there is an increased need for flexibility in the products in the safety-critical market. This need for flexibility puts new requirements on the customization and the upgradability of both the non-safety and safety-critical critical part. The difficulty with this is the large cost in both effort and money of the re-certification of the modified software, which means that companies cannot fully leverage the advantages of modular software system. RECOMP will provide reference designs and platform architectures together with the required design methods and tools for achieving

cost-effective certification and re-certification of mixed-criticality, component based, multi-core systems. The aim of RECOMP is to define a European standard reference technology for mixed-criticality multi-core systems supported by the European tool vendors participating in RECOMP.

Partners of the RECOMP consortium include, among others:

Fundamental Research Projects

AVIACC

Analysis and Verification of Concurrent Critical Programs

FCOMP-01-012244-FEDER-020486 PTDC/EIA-CCO/117590
Funding: 94KEUR (CISTER Funding: 24.1KEUR)

3 years (May 2012 to Apr 2015)

The goal of the project is to extract models from concurrent programs and building an automatic framework for checking (temporal) properties using verification technologies, both static and run-time

MASQOTS

Mobility mAnagement in wireless Sensor networks under QoS constraints using standard and Off-The-Shelf technologies

FCOMP-01-0124-FEDER-014922 PTDC/EEA-TEL/112220/2009
CISTER Funding: 94.8KEUR

42 months (Feb 2011 to Jul 2014)

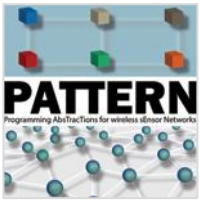
MASQOTS aims at real-time and reliable communications in IEEE 802.15.4/ZigBee (15.4/ZigBee, for short) Wireless Sensor Networks (WSNs) supporting physical mobility. Physical mobility concerns mobile sensor/actuator nodes and node groups (e.g. body sensor networks (BSNs), robots), and also mobile sinks (e.g. gateways, user-interface equipment).

The main objective of this project is to design a real-time and reliable mobility management mechanism for IEEE 802.15.4/ZigBee-based WSNs.

We will build upon the most widespread WSN technologies – the 15.4 and ZigBee protocols and the TinyOS operating system (OS) – for which the research team in this proposal is international leader. OnWorld predicts that in 2012, 88.3% of the WSN units will be standards-based. Freescale reports over 7 million 15.4/ZigBee units sold in 2008 and In-Stat forecasts 292 million units in 2012. TinyOS is the most used OS for WSNs.

MASQOTS will also address some fundamental (not yet solved) problems, such as the ones related to reliable Radio Link Quality Estimation (LQE), efficient and dynamic resource management, reliable and time-bounded handoff and re-association mechanisms and the provision of (simulation, analytical) models/tools for WSN analysis and dimensioning.

PATTERN



Programming AbsTracTions for wireless sEnsor Networks

FCOMP-01-0124-FEDER-028990 PTDC/EEI-SCR/2171/2012
CISTER Funding: 149KEUR

28 months (Jun 2013 to Sep 2015)

In this project, we aim to tackle two critical challenges for the future success of WSN: (i) provide a seamless model for the development of correct applications, whilst (ii) efficiently managing and isolating multiple independent applications.

Our WSN model and framework will seamlessly deploy multiple independent applications on a heterogeneous sensing infrastructure, coordinating computations, packet delivery and data aggregation to reduce overall resource usage. The programming framework is based on a macro programming approach and includes high-level programming abstractions. We plan to co-design the programming framework with adequate design patterns (a widely accepted software engineering approach).

We claim that such developments are crucial for future WSN and will be beneficial in many usage scenarios. This project particularly targets the use-case of modern smart buildings One important aspect of this application domain is that different users might develop them at different times, and it is not practical to merge them into a single application.

REGAIN

Real-time scheduling on general purpose graphics processor units

FCOMP-01-0124-FEDER-020447 PTDC/EIA-CCO/118080/2010
CISTER Funding: 139KEUR

40 months (Apr 2012 to Jul 2015)

Among all processors sold today, 98% are used in embedded computer systems; therefore, catering to this segment is of utmost importance. Moreover, there is a persistent trend in computing that techniques originally developed at the high-end (pipelining, cache-memories, instruction-level parallelism) later propagate to embedded computer systems. Graphics processors are the next technology to do this transition.

Therefore, this project will create a real-time scheduling theory for GPGPUs. This theory will offer (i) a model suited for describing real-time scheduling on GPGPUs, (ii) algorithms for run-time scheduling of tasks using GPGPUs and (iii) algorithms for proving, before run-time, that tasks using GPGPUs meet their deadlines. This project will also test the theory on commercially available GPGPUs.

REHEAT

Real-time scheduling on heterogeneous multicore architectures

FCOMP-01-0124-FEDER-010045 PTDC/EIA-CCO/105716/2008
CISTER Funding: 130KEUR

3 years (Feb 2010 to Jan 2013)

Parallel processing platforms are spreading at an unprecedented rate. Traditionally, parallel processing platforms were used to reduce the execution time of a large computational job such as predicting the weather but now they are also used in low-end systems and embedded real-time systems thanks to the availability of multicore processors. And those systems are often comprised of a large number of independent tasks. Designers are well-aware that processing units specialized for a specific function can offer a significant performance boost. Consequently, heterogeneous multicores now enjoy a period of widespread use. Virtually all major semiconductor companies are offering or have declared plans to offer heterogeneous multicores.

This project aims to create provable good real-time scheduling algorithms for heterogeneous multicores.

RePoMuc

Real-time Power management on partitioned MultiCores

FCOMP-01-0124-FEDER-015050 PTDC/EIA-EIA/112599/2009
CISTER Funding: 106KEUR

3 years (Feb 2011 to Jan 2014)

The fundamental objective of the RePoMuC project to provide a methodology for real-time power-management in Multicores, considering: 1. the non-linear behaviour of dynamic frequency and voltage scaling (DVFS) on execution-time and energy, 2. pre-emption delays, and 3. memory bus contention Particular focus will be given to demonstrate with a real-world implementation the practicality and limitations of the proposed methodology. The approach I intend to take is to build on successful experience of the group in the areas of DVFS power management, real-time multiprocessor scheduling and temporal isolation. The issues of DVFS behaviour, pre-emption delays, and memory bus contention have a fundamental communality in the sense that they are all tightly coupled to the amount of memory traffic.

REWIN

Real-Time Guarantees in Wireless Sensor Networks

FCOMP-01-0124-FEDER-010050 PTDC/EIA-CCO/109027/2008
CISTER Funding: 68KEUR

3 years (Feb 2010 to Jan 2013)

A class of WSN applications require timely response to events. For example, in a smart nursing home WSN scenario, it is necessary to guarantee that life-threatening events such as heart-attacks are communicated to doctors within a bounded time. The ability to support real-time applications is fundamental to the advancement of capabilities of WSN, and is the motivation for this proposed research. Since communication is an integral part of WSN, the performance of WSN is mainly determined by the quality and capacity of the wireless channel. The limited previous research that exists is insufficient to guarantee (with mathematical proofs) a low delay for disseminating the occurrence of rare but critical events, such as the heart-attack mentioned above. This project, we will develop methods to offer hard real-time guarantees to individual real-time flows over multi-hop WSN of arbitrary node deployments and arbitrary traffic pattern. These methods will guarantee a small delay for disseminating the occurrence of critical events.

SMARTS

Slack Management in Hierarchical Real-Time Systems

FCOMP-01-0124-FEDER-020536 PTDC/EIA-CCO/121904/2010
CISTER Funding: 158KEUR

42 months (Apr 2012 to Sep 2015)

Most of modern computing systems are embedded with the physical environment. When such embedded systems are additionally subject to temporal constraints they are termed real-time systems.

There are a number of relevant trends in real-time systems: the complexity of such systems increases dramatically, often leading to integration of subsystems from various vendors; real-time and best effort applications may share the processor on a given device; the software on such systems may be subject to change leading to dynamic real-time systems.

A widely accepted design paradigm for such complex systems is component-based engineering in which 1) the system is first decomposed into simpler and smaller applications, 2) applications are independently designed and analysed, and 3) applications are composed together to generate the system. Depending on how the applications are grouped together for composition, the resulting system can be represented as a tree of applications; each parent-children pair denotes a composition where the child-applications were composed together to form the parent-application.

Within this project, we will: propose to investigate a comprehensive reclamation of all slack in a hierarchical system; investigate the impact of preemption, integrate pre-emption estimation techniques and provide a framework for alternative policies. Finally, we will explore how the developed techniques can be applied in a multicore setting.

For this we will build on the work of the ViPCore project (PTDC/EIA-CCO/111799/2009) also executed in CISTER, which in turn builds in among other things on [11, 27]. The multicore development will run in parallel to the other activities once the initial work on uniprocessors have been identified.

SENODs

Sustainable ENergy-Optimized Datacenters

FCOMP-01-0124-FEDER-012988 CMU-PT/SIA/0045/2009
Funding: 292KEUR (CISTER Funding: 219KEUR)

39 months (Oct 2010 to Dec 2013)

Data centres increasingly constitute a critical backbone of the worldwide information technology (IT) infrastructure, forming the server infrastructure for search engines, mail servers, e-commerce, data warehousing and other cloud computing functions. Thousands of data centres operate across the world occupying various millions of square meters. While such data centres generally target large-scale virtual IT services, the design, construction and operation of data centres (i) depend on cyber-physical infrastructure with major power and cooling requirements, (ii) incur significant energy costs, and (iii) can lead to significant economic and societal impact from the failures of physical subsystems. In fact, power and cooling in a data centre cost more than the IT equipment supported. As a result, data centres face an emerging crisis. The SENODs (Sustainable ENergy-Optimized Datacenters) project will rectify that by: (i) using ultimate distributed sensing technologies to provide fine-grained monitoring of power consumption, cooling and data centre environmental variables to identify, model, analyse and optimize energy costs; (ii) developing intelligent layout optimization algorithms that offer recommendations regarding placement of new servers so as to minimize local hotspots and improve energy efficiency; (iii) providing support for alerts and notifications of actual or pending failures in cooling and other infrastructure equipment to gracefully shut down some or all of centre operations; (iv) online capacity and workload management that allows dynamic reallocation of computing loads driven by energy and cost minimization.

Partners of the SENODs consortium include:

Smartskin

Densely Instrumented Physical Infrastructures

FCOMP-01-0124-FEDER-020312 PTDC/EEA-ELC/121753/2010
CISTER Funding: 141KEUR

3 years (Mar 2012 to Feb 2015)

Although the information technology transformation of the 20th century appeared revolutionary, a bigger change is on the horizon. The term Cyber-Physical Systems (CPS) has come to describe the research and technological

effort that will ultimately allow the interlinking of the real-world physical objects and the cyberspace efficiently. The integration of physical processes and computing is not new.

Embedded systems have been in place for a long time and these systems often combine physical processes with computing. The revolution will come from massively networked embedded computing devices, which will allow instrumenting the physical world with pervasive networks of sensor-rich embedded computation.

In this project we intend to develop techniques and technologies that allow performing scalable and efficient data processing in large-scale dense cyber-physical systems. This is yet an unsolved problem. The major novelty of this proposal is effectively in the co-design of distributed algorithms for sensor data processing and underlying networked distributed computing systems with corresponding resource management schemes such that the utilization of resources is low.

VipCore

Virtual Processor-based Multicore Scheduling

FCOMP-01-0124-FEDER-015006 PTDC/EIA-CCO/111799/2009
CISTER Funding: 111KEUR

40 months (Feb 2011 to Jun 2014)

Scheduling on multicores is a much harder problem than those studied under single processor scheduling theories, largely because of the inherent non-parallelism in workload tasks. Although a multicore platform may execute different tasks from a workload at the same time, it is typically not allowed to execute the same task on more than one core simultaneously. This project plans to research multiprocessor frameworks and platforms to tackle these issues. One important concept is the notion of virtual processors, which allow to use a three-step scheduling strategy: partitioning of workload tasks and assigning virtual processors to each partition, scheduling of tasks on virtual processors within each cluster, and scheduling of virtual processors on the physical cores. Another important concept is the notion of pJobs, which allow tasks to be executed in parallel in the physical cores, increasing the potential parallelism of applications. The project will also research into architectures and platforms for supporting these concepts, and the underlying resource sharing paradigms.

Highlights 2013

www.cister.isep.ipp.pt/news

January

CISTER wraps up European Network of Excellence in Cooperating Objects

CISTER/INESC-TEC researchers Filipe Pacheco and Mário Alves participated in the final Review Meeting of FP7 European Network of Excellence in Cooperating Objects (CONET) in Brussels, Belgium, on the 29/JAN/2013.

Filipe presented the major outcomes of the SDP (Scalable Data Processing) research cluster where CISTER's unique in-network data processing algorithms are combined with knowledge from researchers in Dublin (NUIG DERI), Duisburg (UDE) and Cyprus (UCY). Results were published in top journals and the cluster received the CONET's PhD Best Thesis Award.

Mário presented the WP5 (Spreading of Excellence) results and the COTS4QoS research cluster. The COTS4QoS research cluster produced excellent R&D results and a set of planning and engineering tools that widely used by the international community. This cluster also produced relevant standardization, outreach and exploitation results.

The Project Officer praised the projects results and the congratulated the participants for the successful conclusion of the undertaking. Since 2008 there were more than 350 papers with CONET label, 4 editions of EWSN conference were sponsored, a series of Springer Briefs was produced and also two special sections in journals, and three Summer Schools were organized.

The CONET Network of Excellence addressed the research and technological effort that will ultimately efficiently allow interlinking the real world physical objects and cyberspace, generally coined as "Cooperating-Objects" or "Cyber-Physical Systems (CPS)".

Expert Seminar on Multicore Enablement for Embedded and Cyber Physical Systems

In the last week of January CISTER researcher Stefan M. Petters attended the by-invitation-only seminar on Multicore Enablement for Embedded and Cyber Physical Systems at Schloss Dagstuhl in Germany.

The workshop was organised by Andreas Herkersdorf (TU Munich), Michael Paulitsch (EADS-Innovation Works), and Michael Hinchey (University of Limerick). It brought together researchers from industry and academia to discuss the challenges faced in and solutions proposed for the deployment of multicore processors in embedded systems. Stefan in this context presented CISTER research on application mapping in NoC based manycores and together with Rene Graf (Siemens AG) he led a working group on "Certification of Safety Critical

Multicore Systems: Challenges and Solutions".

The various seminars at Dagstuhl are mostly designed to tackle a specific problem by bringing together a group of researchers with complementary skills and its results often serve as focal point to develop input to the national and European policy makers to shape future research agendas. In line with this spirit, the attendees of this seminar has varying background, spanning the area vertically from hardware design, operating systems, up through to middleware and programming model and language issues, as well as horizontally the automotive, aerospace, industrial automation, and medical systems industry.

Positive results for CISTER in the European FP7 Call 10

Within the scope of the on-going efforts by CISTER to participate in the European R&D calls, last January CISTER participated in several initiatives to tackle the FP7 Call 10 (with projects submitted last January 17).

In that call, CISTER addressed in particular Objective ICT-2013.3.4 (Advanced computing, embedded and control systems), which intends to "combine and expand Europe's industrial strengths within embedded and mobile computing and in control of networked embedded systems".

The results of that call have been recently known, and provide a very positive outcome for the research centre activities.

CISTER-led project proposal P-SOCRATES (Parallel Software Framework for Time-Critical many-core Systems), which targeted outcome c) "Exploiting synergies and strengths between computing segments", received very good marks, and has been ranked within the first group of proposals, entering now the final negotiation phase. The project has a budget of 3.6 M€, and a foreseen EC contribution of 2.7 M€. CISTER has the largest share of this contribution, with around 550 K€ of European contribution.

Although not selected for funding, another proposal where CISTER participated, the CHORAL large Integrated Project, also received positive comments and received the same score as another proposal that was selected for negotiations. CHORAL addressed outcome b) "Control in embedded systems with mixed criticalities sharing computing Resources", and involved partners such as Universities of Trento and Pisa (Italy), KTH (Sweden), INRIA (France), NLR (Netherlands), Piaggio (Italy), ABB (Sweden) and Boeing (Spain).

This project focused on addressing mixed-criticality challenges in application domains such as factory automation and traffic management within airports. The positive comments received are being considered and the consortium is continuing to work on the proposal to tackle the forthcoming calls of Horizon 2020.

SENODs on its Way to Large-Scale Deployment

One more step to the large-scale deployment of SENODs with the ongoing preparation of a new pilot deployment at PT-Picoas, where an entire data-center room will be monitored with an unprecedented sensing granularity. This pilot is planned to kickoff in next February.

In the SENODs project (Sustainable ENergy-Optimized Datacenters), CISTER/INESC TEC researchers are working towards constructing integrated solutions to address both the cyber and physical challenges posed by the energy consumption, cooling, and operational needs of large-scale datacenters. The SENODs project consortium is lead in Portugal by CISTER and in the USA by Carnegie-Mellon University, and the other academic partner is FEUP in Portugal. The project is industrially driven by major Portuguese corporation Portugal Telecom (PT), which is undergoing a major overhaul of its datacenter facilities with the construction of a new, very large, and state-of-the-art datacenter in Covilhã.

February

Researchers Vincent Nélis and Stefan M. Petters Represent CISTER in Final RECOMP Project Meeting

CISTER Researchers Stefan M. Petters and Vincent Nelis participated in the final RECOMP project meeting and general assembly held in Madrid, on the 5th and 6th of February 2013.

RECOMP is an Artemis-JU project involving 40 participants from industry, SMEs and academic institutions, e.g. EADS, Honeywell, Thales, Infineon and SYSGO. It addresses the certification and recertification of multicore systems. CISTER was contributing broadly in almost all work packages but most heavily and successfully in WP 2 dealing with analytical techniques, as well as the evaluation of certification challenges in WP4.

The general assembly was mainly concerned with the preparation of the upcoming final project review. Overall, the project concluded with substantial progress achieved in the certification of multicore architectures across significant application domains where Europe excels: automotive, aerospace and industrial electronics.

March

SENODs technology is Now Deployed at Portugal Telecom (PT) Datacenter in Picoas, Lisbon

The SENODs team successfully carried out a proof-of-concept deployment at PT-Picoas. This deployment is a a long-lived demonstration of the technology developed within the SENODs project and will enable the analysis of datacenter power and environmental variables to an unprecedented granularity.

PORTUGAL TELECOM

The results from this deployment will mean that Portugal Telecom (PT) will know in much greater detail exactly what the data centre is using, why it is using this and what is the cause of this. Using this data PT will be able to configure the data centre for it to run as efficiently as possible. This proof-of-concept is also the kickoff of other deployments within datacenters owned by PT.

In the SENODs project (Sustainable ENergy-Optimized Datacenters), CISTER/INESC-TEC researchers are working towards constructing integrated solutions to address both the cyber and physical challenges posed by the energy consumption, cooling, and operational needs of large-scale datacenters.

The SENODs project consortium is lead in Portugal by CISTER/INESC-TEC and in the USA by Carnegie-Mellon University the other academic partner in Portugal is FEUP. The project is industrially driven by the major Portuguese corporation Portugal Telecom (PT), which is undergoing a major overhaul of its datacenter facilities with the construction of a new, very large, and state-of-the-art datacenter in Covilhã.

High Profile Academics Descend on Porto for the ECRTS'13 TPC Meeting

March 16 saw more than 30 world-renowned academics gather at CISTER/INESC-TEC for the Technical Program Committee meeting of the 25th Euromicro Conference on Real-Time Systems (ECRTS'13). ECRTS is one of the flagship events of the embedded real-time systems community. It will take place from 9th to 12th of July 2013 in Paris, France and encompass besides the main conference, a set of highly popular targeted Workshops on Operating Systems Platforms, Worst-Case Execution Time, Real-Time Networks, Analysis Tools, and Open Problems in real-time Scheduling, as well as a work-in-progress session for work in early stages of development.

CISTER/INESC-TEC researcher Stefan M. Petters is serving as Technical Program Committee Chair of ECRTS'13. In this function he was leading the TPC meeting. This is an outstanding recognition both for Stefan and the CISTER/INESC-TEC research unit as a whole and is a testament to the excellent work performed in the unit. As reported in the last news, this forms a string of recognitions CISTER/INESC-TEC has received for RTAS 2013, SIES 2013 and RTSS 2013.

ARTEMIS ARROWHEAD Project Kickoff Meeting

The Artemis Arrowhead project will have its kickoff meeting on the 14th of March, during the Artemis Spring event in Brussels.

ARROWHEAD

Arrowhead belongs to the first group of very large Artemis AIPP projects. It has an overall budget of around 90 million Euros, involving most European countries. Besides ISEP (through CISTER/INESC-TEC), the Arrowhead project involves key European industrial players such as Acciona (SP), Airbus Operations (FR), FIAT (IT), Ford (UK), Honeywell (CZ), INDRA (SP), Infineon (AT), NXP (FR), Schneider Electric (FR), STMicroelectronics (IT), and Thales (FR).

The Arrowhead project addresses cooperative automation and is enabled by the technology developed around the Internet of Things and Service Oriented Architectures. The project will provide a technical framework adapted to such systems. Implementation and evaluation will be through through real deployments in various applicative domains: electro-mobility; smart buildings; infrastructures and smart

cities; industrial production; energy production and energy virtual market.

The strategy adopted in the project is based on business and technology gap analysis paired with a market implementation strategy based on end users priorities and long term technology strategies, after, application pilots in real working environments will be implemented. All these strategies will be supported by a common technology framework enabling collaborative automation and closing innovation critical technology gaps, which is tightly linked with an innovation coordination methodology for complex innovation "orchestration".

Celebration of the 60th anniversary of Professor Alan Burns

CISTER/INESC-TEC researchers Stefan M. Petters and Konstantinos Bletsas participated in a one-day workshop titled "Real-time systems: the past, the present and the future". This was held at the University of York, on March 14th, 2013. This one-off event was organised by Prof. Sanjoy K. Baruah (U. North Carolina, USA) and Dr Neil C. Audsley (U. of York, UK) in celebration of the 60th birthday of Professor Alan Burns and in recognition of his contributions to the research community.

Professor Alan Burns is one of the members of the CISTER/INESC-TEC External Advisory Board (EAB). His research interests cover a number of aspects of real-time systems including the assessment of languages for use in the real-time domain, distributed operating systems, the formal specification of scheduling algorithms and implementation strategies, and the design of dependable user interfaces to real-time applications. He has authored/co-authored 450 papers/reports and 15 books.

The Real Time Systems Research Group of the University of York was established in 1990 and since then has undertaken research into all aspects of the design, implementation and analysis of real-time systems. This workshop allowed for discussions to be held between the research institutes involved within the Real Time Systems area.

Project CarCoDe received approval for funding

We are pleased to announce that the CarCoDe project has been approved by the System of Incentives for Research and Technological Development (SI I&DT) of the National Strategic Reference Framework (QREN). Negotiations with the Portuguese Funding Agency, ADI – Agência de Inovação, have now been successfully concluded, and the project is set to start on July 1st.

CarCoDe

CarCoDe (Platform for Smart Car to Car Content Delivery) is an European R&D project, labeled within the ITEA 2 program, with partners such as Cassidian (FR), NXP (FR), Thales C&S (FR), University Paris-East (FR), Easy

Innova (SP), Universiry of Girona (SP) and GM (SP).

As an ITEA labeled project, funding applications are done per country. After the successful funding applications in Spain and France, the European project started last December 2012, with the kickoff meeting taking place this March.

The Portuguese National application was submitted by a Consortium, led by the Mecalbi SME and made up by the partners CISTER/INESC-TEC, Instituto de Telecomunicações, PT Inovação, IPCB and Evoleo Technologies.

CISTER/INESC-TEC is the national contact to the ITEA Consortium.

CarCoDe will develop a software platform for the automotive domain. The aim of this software is to generate a readable traffic service domain which displays all information related to all automotive users (car drivers, truck operators, traffic management planners, etc).

The project leader within CISTER/INESC-TEC is researcher Luis Miguel Pinho.

April

CISTER Researcher Leads the Scientific Program of Top-Tier International Conference

Eduardo Tovar was the Program Chair of the 19th IEEE Real Time and Embedded Technology and Applications Symposium (RTAS 2013), a top tier conference in the area. The conference was held during April in Philadelphia, Pennsylvania, USA, as part of the Cyber-Physical Systems Week (www.cpsweek.org).

The scope of RTAS is defined by its four tracks: Track 1 on Applications, Systems, RTOSs, and Tools; Track 2 on Applied Methodologies and Foundations, that is, on basic methodologies and algorithms that are applicable to real systems to solve specific problems; Track 3 on Wireless Sensor Networks; and Track 4 on Hardware-Software Co-design, including design methodologies and tools for hardware/software integration. Papers submitted to all tracks were required to clearly define motivating application examples and include a section reporting experimental results with a real implementation of the proposed system, or showing the applicability to an industrial case study or working system.

One of the highlights of this year's RTAS was the Industrial Session, which included talks by various industrialists on case studies, design methodologies, tools, deployment experiences and industry challenges in various application domains. This session included speakers from Siemens, General Motors, Mathworks, Honeywell, Emerson, United Technologies and National Instruments.

CISTER on the Spotlights of a Television Science and Technology Dissemination Show

CISTER researcher Mário Alves participated in the official presentation "100 segundos de ciência" (100 seconds of science), a joint venture between RTP, FCT and the Portuguese Commission of UNESCO.

"100 segundos de ciência" is a series of short programs with each program addressing cutting edge scientific research that is "Made in Portugal". It has started with 10 different episodes which were shown on RTP2 (Portuguese television) from the 22nd April. The idea is to disseminate science in a straightforward way, giving special emphasis to the practical results, applications and usefulness for the general public, aiming to close the gap between the scientific community and general society. One of the 10 programs included reports on the work done at CISTER on wireless sensors networks and applications, particularly the work driven from the EMMON project (which was led by Critical Software) and also included some reports on the ongoing work under the SENODS project (with Portugal Telecom). The programs have been broadcast on RTP2 and will soon be repeated on RTP1, RTP International (with subtitles) and RTP Africa.

They are now available on-line at http://media.rtp.pt/blogs/cienciaeambiente/

The Minister of Science and Education, the President of FCT and the President of the National Commission of UNESCO were also present at this event, among other invited participants.

May

TACLe Panel of Experts Workshop on Programming Models for Parallel Architectures

The EU COST Action on Timing Analysis on Code Level (TACLe) held its first Focussed Workshop at CISTER on the 21st of May. A COST Action is a funding mechanism which focuses on fostering exchange between researchers working on different research projects on national and international level on thematic commonalities. The TACLe COST Action involves researchers from 17 countries and such renown Universities as the University of York, UK, Mälardalen University, Sweden, or TU Vienna, Austria, to name but a few.

The focussed meeting organised by CISTER's Stefan M. Petters targeted parallel programming models in real-time systems and consequently their impact on code level timing analysis. It was structured around a set of talks by Ian Gray (University of York), Luís Miguel Pinho (CISTER), Raimund Kirner (University of Hertfordshire) Tullio Vardanega (University of Padua) interspersed with ample discussion time. Besides noteworthy speakers, the meeting was attended by PhD students from England, Sweden, Italy and a substantial number of CISTER researchers.

PC Co-Chair of the 26th International Conference of Architecture of Computing Systems (ARCS 2014)

CISTER Researcher Eduardo Tovar is to serve as Program Co-chair of the ARCS 2014 Architecture of Computing Systems conference to be held the University of Luebeck (Germany) on February 25-28, 2014.

The ARCS series of conferences has over 30 years of tradition reporting top notch results in computer architecture and operating systems research. The focus of the 2014 conference will be on embedded computer systems connecting computing with the physical world. Like the previous conferences in this series, it continues to be an important forum for computer architecture research.

ARTEMIS/FP7 CONCERTO Project Kick-Off Meeting

The Artemis CONCERTO project had its kickoff meeting on 13th and 14th of May, 2013 in Pisa, Italy, where CISTER's researchers Eduardo Tovar, Vincent Nelis, Geoffrey Nelissen and Gurulingesh Raravi participated.

CONCERTO will address emerging embedded systems platforms harnessing new heterogeneous, multicore architectures to enable the next generation of powerful mission-critical applications. The applicability of the CONCERTO solutions will be validated in the aerospace, telecoms, automotive, petroleum and medical industrial domains.

CISTER will have a bold participation in the CONCERTO project. CISTER will be central to the success of one of the main objectives of CONCERTO, which is extending the multicore domain the model driven engineering approach for critical software development that resulted from the recently finished CHESS FP7/Artemis project.

Besides ISEP (through CISTER/INESC-TEC), the CONCERTO project involves key industrial players such as Intecs (IT), Thales (FR), Atego (FR), EADS (FR), Aicas (DE), The Open Group (UK), Oilfield Technology Group (NO) and Critical Software (PT). From the EADS group both Airbus (aviation) and Astrium (satellites) are participating. CONCERTO is a 10 Million Euros cost project, out of which 4 Million Euros of funding (both EU and National funding). The total funding for ISEP will be 375 KEuros.

June

SENODS Project Evaluation

Following similar events from previous years, the Carnegie Mellon Portugal Program, funded by FCT conducted the annual project review last June 18th, in the Pavilhão do Conhecimento, Lisbon.

The project review consisted of an overview presentation of the research projects made to an Evaluation Committee, composed of specialists in the area. Representatives of CISTER/INESC-TEC and of the industrial partner involved in the SENODs project (Sustainable ENergy-Optimized Datacenters), participated in this meeting. The efforts carried out under the SENODS project deserved excellent feedback by the Evaluation Committee, and the project results were considered very relevant by the industry partner.

First CISTER Industrial Workshop

CISTER organized the 1st Industrial workshop CiWork 2013 on June 18. The aim of the CISTER Industrial Workshop is to bring together researchers and practitioners from within industry and academia and provide them with a platform to report on recent advances and developments in the newly emerging areas of real-time and embedded technologies, as well as actual and potential applications to industrial systems.

Besides a poster session presenting CISTER's work of interest to the industrial attendees, several companies presented their view on the real-time embedded systems challenges and opportunities, namely: Tomorrow Options, Micro I/O, Critical Software, Edisoft, Critical Materials, ISA, Evoleo and Aavanz.

CISTER hosts SIES'2013, the 8th IEEE International Symposium on Industrial Embedded Systems

CISTER organized and hosted the 8th IEEE International Symposium on Industrial Embedded Systems on 19 - 21 June 2013 in Porto, Portugal. SIES is one of the leading events in the area of real-time embedded systems sponsored by the IEEE. CISTER researchers also played an instrumental role within the program committee, where CISTER researchers acted as General Co-Chair, Publication chair and Finance chair.

Besides an interesting program with several talks from researchers around the world, there were three keynote speakers. Rolf Ernst: Automotive Communication - From Buses to Switched Networks; Michael Paulitsch: Dependable and secure computing and networks in aerospace - the past, the present and a glimpse into the future; Chenyang Lu: Real-Time Wireless Control Networks for Cyber-Physical Systems.

July

CISTER Researcher Leads the Scientific Program of ECRTS 2013

Stefan M. Petters was the Program Chair of the 25th Euromicro Conference on Real-Time System (ECRTS'13). ECRTS is one of the flagship events of the embedded real-time systems community and it took place from 9th to 12th of July 2013 in Paris, France.

August

CISTER/INESC-TEC Scores the Best Paper Award at RTCSA 2013

The IEEE Conference on Real-Time Computing Systems and Applications (RTCSA) is a well reputed and highly competitive event. This year the conference was held on 19-21 August in Taipei, Taiwan and saw a strong presence by CISTER researchers, who managed to get six papers accepted to this conference.

The best paper award of the real-time systems track was assigned to the paper "Global Fixed Priority Scheduling with Deferred Pre-emption", which was a collaborative work by the University of York (Robert Davis and Alan Burns), University of Modena (Marko Bertogna) and CISTER (Jose Marinho, Vincent Nelis, and Stefan M. Petters). This is a truly remarkable achievement for the collaborative efforts of CISTER and CISTER researchers.

Co-located with RTCSA 2013 was the 1st IEEE International Conference on Cyber-Physical Systems, Networks, and Applications (CPSNA 2013).

CISTER was also presenting one paper in this venue bringing the total participation of CISTER to these two conferences to seven accepted papers with one best paper award which once more demonstrated the strong presence of CISTER in the community.

September

CMU Portugal Working Session "Converting Technology into Products and Services"

On September 18th, CISTER hosted a working session of the CMU Portugal program on "Converting Technology into Products and Services". The session counted with Dr. Nikhil Balram, President and CEO of Ricoh Innovations Corporation (http://rii.ricoh.com). Dr. Balram has large experience in creating new ventures, by managing the integration of technology, user experience and business expertise. Dr. Balram is also adjunct professor of electrical engineering at Carnegie Mellon University, visiting professor of vision science at the University of California, Berkeley, and a guest professor at the Indian Institute of Technology (IIT) in Gandhinagar, India.

During the session, the PIs of Portugal CMU ongoing projects had the opportunity to present the main research outcomes of each project and discuss with Dr. Balram about the next steps in order to convert the developed technologies into commercial products and services.

Besides Dr. Nikhil Balram, the session also counted with João Claro (CMU-Portugal director), João Paulo Cunha, João Barros, Nuno Pereira, Vitor Grade Tavares, Sara Brandão, Alexandra Carvalho Vieira and Eduardo Tovar.

Thesis Proposal Defense of CISTER/INESC-TEC Student in the CMU Portugal Program

CISTER PhD student researcher, Vikram Gupta, visited Carnegie Mellon University (CMU), Pittsburgh, from Aug 16th to Sep 20th to continue the joint research with Prof. Raj Rajkumar.

Vikram Gupta successfully presented his Thesis Proposal entitled "On the Optimization of Multiple Applications for Sensor Networks". The thesis proposal presentation was attended and evaluated by Prof. Eduardo Tovar, along with Prof. Raj Rajkumar, Prof. Peter Steenkiste and Prof. Anthony Rowe (faculty members from CMU).

Two new Booklets authored by CISTER/INESC-TEC Researchers

Two new booklets in the Springer Briefs in Electrical and Computer Engineering have been published with strong participation of CISTER researchers. These books are a corollary of the work that has been performed in the last few years in the area of wireless sensor networks, resulting particularly from the collaborative efforts in the EMMON, CONET, SENODS and MASQOTS projects.

The first booklet, titled “IEEE 802.15.4 and ZigBee as enabling technologies for low-power wireless systems with quality-of-service constraints” unveils the most important characteristics of IEEE 802.15.4 and ZigBee and how they can be used for engineering Cooperation Objects systems and was authored by Stefano Tennina, Anis Koubâa, Roberta Daidone, Mário Alves, Petr Jurcik, Ricardo Severino, Marco Tiloca, Jan-Hinrich Hauer, Nuno Pereira, Gianluca Dini, Mélanie Bouroche and Eduardo Tovar.

The second booklet titled “Radio link quality estimation in low-power wireless networks” provides a comprehensive survey on related work for radio link quality estimation of Cooperation Objects and was authored by Nouha Baccour, Anis Koubâa, Claro Noda, Hossein Fotouhi, Mário Alves, Habib Youssef, Marco Antonio Zuniga, Carlo Alberto Boano, Kay Roemer, Daniele Puccinelli, Thiemo Voigt, and Luca Mottola.

Invited Talk at Spanish Real-Time Systems Symposium

CISTER Researcher Luis Miguel Pinho gave an invited talk in the Spanish Real-Time Systems Symposium, which took place September 18-19, in Madrid. This symposium was one of the parallel tracks of the Spanish Congress on Informatics, an event with around 700 attendees.

The talk, titled "Real-Time Parallel Models" presented some of the challenges of parallel real-time models, focusing in particular in work being carried out at CISTER in the integration into the real-time domain of techniques from the high-performance area, such as work-stealing scheduling and parallel programming models.

This was also an opportunity for networking with other researchers in the areas of real-time and embedded systems, and in particular with institutions that CISTER regularly collaborates with, such as Universidad Politécnica de Madrid, Universidad de Cantabria and Universidad Politécnica de Valencia.

CISTER/INESC-TEC joins ISEP in the 1st ISEP Alumni Gathering

On the 21st of September, ISEP has promoted a reception for all its alumni. This event joined together more than 100 alumni in a joyfully and friendly environment.

After lunch all alumni had the possibility of visiting ISEP's labs, departments and research centers. CISTER also joined ISEP's efforts by opening our doors to some of them, mostly from Informatics and Electrotechnical engineering. Several of our members lead them on a visit to our facilities showing our new (for them) installations and our progress over the last years. The visit was organized around a set of posters related to most of our current and past projects. At the end of the visit there was a cheerful discussion on ISEP's progress during the last few years.

October

P-SOCRATES: FP7 European Project led by CISTER/INESC-TEC Just Started

P-SOCRATES (Parallel SOftware framework for time-CRitical mAny-core sysTEmS) is an FP7 funded project aiming to develop new techniques for exploiting the massively parallel computation capabilities of next-generation many-core embedded platforms in a predictable way.

These platforms are well positioned for intercepting the increasingly convergence of High-Performance Computing (HPC) and Embedded Computing (EC) domains need for predictable high-performance, allowing HPC and EC applications to be executed on efficient and powerful heterogeneous architectures integrating general-purpose processors with many-core computing fabrics.

P-SOCRATES

P-SOCRATES will tackle this important challenge by merging leading research groups from the HPC and EC communities. The time-criticality and parallelization challenges common to both areas will be addressed by proposing an integrated framework for executing workload-intensive applications with real-time requirements on top of next-generation commercial-off-the-shelf (COTS) platforms based on many-core accelerated architectures. The project will investigate new HPC techniques that fulfil real-time requirements. The main sources of indeterminism will be identified, proposing efficient mapping and scheduling algorithms, along with the associated timing and schedulability analysis, to guarantee the real-time and performance requirements of the applications.

The project partners include as research institutions, besides ISEP, the Barcelona Supercomputing Centre (Spain), the University of Modena (Italy) and the Swiss Federal Institute of Technology Zurich (Switzerland). The industrial partners of the project include ATOS (Spain) and the SMEs Evidence (Italy) and Active Technologies (Italy). The project partners are supported by an industrial advisory board, which includes well-known multi-national

companies including STMicroelectronics, IBM, Honeywell and Airbus.

Besides overall coordination and technical management, CISTER will be also deeply involved in the parallelism to real-time activity, leading in particular the Timing and Schedulability analysis work package.
The project started this October with the kick-off meeting taking place October 21-23 in Barcelona, Spain. The first two days were dedicated to discuss the technical advancements of the project, being the third day dedicated to a meeting of the project partners with the Industrial Advisory Board. The CISTER team at the meeting was integrated by Luis Miguel Pinho (Project Coordinator), Vincent Nélis, Patrick Yomsi and José Carlos Fonseca.

P-SOCRATES is a project in the scope of the call 10 of the FP7 program, under the Information objective "Advanced Computing Embedded and Control Systems". The project will run for 3 years (until September 2016) with a total budget of 3.6 M€, being 2.76 M€ the EU contribution.

Best Presentation Award at RTNS 2013

CISTER's researchers had a significant participation at the 21st International Conference on Real-Time Networks and Systems – held in Sophia Antipolis, France, October 16-18, with cutting edge research being presented in the areas of many-cores and network-on-chip, energy consumption, mixed criticality and multiprocessor scheduling. Notably CISTER received the Best Presentation Award for the paper entitled "Feasibility intervals for homogeneous multicores, asynchronous periodic tasks, and FJP schedulers" authored by Vincent Nelis, Patrick Meumeu Yomsi and Joël Goossens, which was presented by Vincent Nelis.

European Project Proposal to Head for Negotiation Phase

The effort developed by CISTER/INESC-TEC in the last open call for research projects in the strategic ARTEMIS initiative is now giving its results as one of the project proposals is well headed into negotiations regarding its funding and approval. It is expected that the project can start early 2014.

The project, EMC2 (Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments) is an Artemis Innovation Pilot Project (AIPP) large project involving many large industrial partners, such as EADS, Thales, Infineon Technologies, Ericsson, BMW, Volvo, Philips Healthcare or Siemens.

The CISTER team in the project, lead by researcher Eduardo Tovar, will be involved in several of the research activities of the project, namely In "Executable Application Models and Design Tools for Mixed-Critical, Multi-Core Embeddded Systems" , "Dynamic Runtime Environments and Services" and "Multi-core Hardware Architectures and Concepts, and in two of the Living Labs (use cases).CISTER and Critical software lead a use case in the automotive area, being CISTER also involved in an avionics use case led by EADS.

CISTER/INESC-TEC Researcher Successfully Defends His PhD

Paulo Baltarejo Sousa, a long-time CISTER researcher has successfully defended his PhD titled "Real-Time

Scheduling on Multi-core: Theory and Practice" on the 29th of October at Faculdade de Engenharia da Universidade do Porto.

The exam committee was Doutor Eugénio da Costa Oliveira, Professor Catedrático da FEUP Doutor Robert Davis, Senior Research Fellow in the Real-Time Systems Research Group, University of York, UK; Doutor Tommaso Cucinotta, Researcher at Alcatel-Lucent Bell Labs in Dublin, Ireland; Doutor José Manuel de Sousa de Matos Rufino, Professor Auxiliar do Departamento de Informática da Faculdade de Ciências da Universidade de Lisboa; Doutor Eduardo Manuel Medicis Tovar, Professor Coordenador do Departamento de Engenharia Informática do Instituto Superior de Engenharia do Porto e Investigador do CISTER-ISEP (Orientador); Doutor Pedro Alexandre Guimarães Lobo Ferreira Souto, Professor Auxiliar do Departamento de Engenharia Informática, Faculdade de Engenharia da Universidade do Porto.

November

Successful Review of European Project ENCOURAGE

CISTER researchers Luis Miguel Pinho and Michele Albano, participated in the 2nd of October in the second year review meeting of the ENCOURAGE project, which took place in the University of Aalborg, Denmark. The meeting was bracketed by internal consortium meetings, for review preparation (Oct 1st) and follow-up activities (Oct 3rd).

The ENCOURAGE project, of the FP7/ARTEMIS Embedded Computing Systems Initiative, aims to develop embedded intelligence and integration technologies that will directly optimize energy usage in buildings with renewable energy and enable active participation in the future smart grid environment.

In the ENCOURAGE project, CISTER is leader of the WP8 Work package (exploitation, dissemination and standardization) and of the T2.3 task, responsible for defining the ENCOURAGE architecture. During this second year, CISTER also had to take the role of responsible for the specification and development of the ENCOURAGE middleware (and in particular of its messaging system), after the funding problems of the initially foreseen partner.

The proactive actions of CISTER in solving this setback, and the quality of the performed work (done by the CISTER team Luis Ferreira, Michele Albano and César Teixeira), was explicitly commended by the Artemis-JU Project Officer in the review summary, particularly as it allowed a very smooth integration process of all ENCOURAGE modules.

The results of this review are successful, as the reviewers provided a positive feedback to the project work, accepting all technical deliverables submitted. In particular the reviewers appraised the demonstration of some of the project results in the demo site of a private house near Aalborg, and of the energy management tools.

In the follow-up meeting, the project consortium set the objectives and planned activities for the next Milestone, where further

demonstrations of the project results and integration activities will be performed at the Terrassa campus in Barcelona, Spain.

December

Another ARTEMIS Project approved for 2014

DEWI (Dependable Embedded Wireless Infrastructure), another ARTEMIS project where CISTER participates was approved. This is another result of the effort developed by CISTER in the last open call for research projects in the strategic ARTEMIS initiative. DEWI is scheduled to start March 2014 and EMC2 (Embedded multi-core systems for mixed criticality applications in dynamic and changeable real-time environments) an Artemis Innovation Pilot Project (AIPP) in April 2014.

DEWI envisions to significantly foster Europe's leading position in embedded wireless systems and smart (mobile) environments such as vehicles, railway cars, airplanes and buildings. Each of these environments is reflected as a domain in the project, and CISTER's main work is in the Aeronautics domain (SP2), led by CISTER researchers. CISTER is also involved in management and architectural work in the Interoperability domain (SP6) that is responsible for finding commonalities between the several application domains. DEWI is also a success case as it has the biggest industrial Portuguese participation in an Artemis project. Besides CISTER, the project involves Critical Software, Critical Materials and GMV.

Wireless Workshop @Airbus Group

CISTER researcher Nuno Pereira has given a talk about the ongoing efforts on developing a dense WSN for Active Flow Control at the Airbus Group (formerly EADS) Wireless Workshop in Munich, Germany.

In aeronautics, wireless communication is considered one of the enablers of efficient maintenance; it will reduce the configuration effort, and is a means to provide new services to passengers and operators. The Airbus Group Wireless Workshop brought together experience from the Airbus Group and other industries, with the aim of providing an insight into upstream research on wireless technologies and its applicability. The audience of the workshop was composed of representatives from Airbus Group business units, other industries, and academia.

Publications

www.cister.isep.ipp.pt/docs

Thesis

1. Sousa, P, "Real-Time Scheduling on Multi-core: Theory and Practice", PhD Thesis, Faculdade de Engenharia da Universidade do Porto. 29, Oct, 2013. Porto, Portugal.
2. Moreira, D, "Fast mobility support in low-power wireless networks: smart-HOP over RPL/6LoWPAN", Master Thesis, Instituto Superior de Engenharia do Porto. 11, Jul, 2013. Porto, Portugal.

Books & Book Chapters

3. Tennina, S, Koubâa, A, Daidone, R, Alves, M, Jurcik, P, Severino, R, Tiloca, M, Hauer, J, Pereira, N, Dini, G, Bouroche, M, Tovar, E, "IEEE 802.15.4 and ZigBee as enabling technologies for low-power wireless systems with quality-of-service constraints", Springer Lecture Notes in Electrical Engineering. Oct 2013, 97 pages.
4. Baccour, N, Koubâa, A, Noda, C, Fotouhi, H, Alves, M, Youssef, H, Zuniga, M, Boano, C, Roemer, K, Puccinelli, D, Voigt, T, Mottola, L, "Radio link quality estimation in low-power wireless networks", Springer Lecture Notes in Electrical Engineering. Jul 2013, 147 pages.
5. Alam, M, Albano, M, Radwan, A, Rodriguez, J, "Throughput Fairness Analysis of Reservation Protocols of WiMedia MAC", Chapter in Green Communication for 4G Wireless Systems, River Publishers, Edited: S Mumtaz. Mar 2013, pp 47-61. Aalborg, Denmark.
6. Alam, M, Albano, M, Radwan, A, Rodriguez, J, "Context Based Node Discovery Mechanism for Energy Efficiency in Wireless Networks", Chapter in Green Communication for 4G Wireless Systems, River Publishers, Edited: S. Mumtaz. Mar 2013, pp 27-45. Aalborg, Denmark.

Journal Papers

7. Koubâa, A, Jamaa, M, "Taxonomy of Fundamental Concepts of Localization in Cyber-Physical and Sensor Networks", Wireless Personal Communications (WiPersComm), Springer. Sep 2013, Volume 72, Issue 1, pp 461-507.
8. Santos-Jr, J, Lima, G, Bletsas, K, "Efficient schedulability tests for real-time embedded systems with urgent routines", Design Automation for Embedded Systems, Springer US. Aug 2013.
9. Albano, M, Rodriguez, J, Hadzic, S, "Use of negative information in positioning and tracking algorithms", Telecommunication Systems: Special Issue on Mobility Management in Future Internet, Springer US. Jul 2013, Volume 53, Issue 3, pp 285-298.
10. Nicolis, S, Fernández, J, Pérez-Penichet, C, Noda, C, Tejera, F, Ramos, O, Sumpter, D, Altshuler, E, "Foraging at the Edge of Chaos: Internal Clock versus External

Forcing", Physical Review Letters (PhysRevLett), American Physical Society. 27, Jun, 2013, Volume 110, Issue 26, pp 268104-4. U.S.A..
11. Raravi, G, Andersson, B, Bletsas, K, "Assigning Real-Time Tasks on Heterogeneous Multiprocessors with Two Unrelated Types of Processors", Real-Time Systems (RTS), Springer. Jan 2013, Volume 49, Issue 1, pp 29-72.

Conference/Workshop Papers

12. Marinho, J, Nélis, V, Petters, S, Bertogna, M, Davis, R, "Limited Pre-emptive Global Fixed Task Priority", 34th IEEE Real-Time Systems Symposium (RTSS), IEEE. 6, Dec, 2013. Vancouver, Canada.
13. Pedro, A, Pereira, D, Pinho, L, Pinto, J, "Logic-based Schedulability Analysis for Compositional Hard Real-Time Embedded Systems", 6th International Workshop on Compositional Theory and Technology for Real-Time Embedded Systems (CRTS 2013). 3, Dec, 2013. Vancouver, Canada.
14. Garibay-Martínez, R, Nelissen, G, Ferreira, L, Pinho, L, "Task Partitioning and Priority Assignment for Hard Real-time Distributed Systems", 2nd International Workshop on Real-Time and Distributed Computing in Emerging Applications (REACTION 2013). 3, Dec, 2013. Vancouver, Canada.
15. Loureiro, J, Gupta, V, Pereira, N, Tovar, E, R., R, "XDense: A Sensor Network for Extreme Dense Sensing", 34th IEEE Real-Time Systems Symposium (RTSS 2013). 3 to 6, Dec, 2013, Work-In-Progress Session.
16. Santos-Jr, J, Lima, G, Bletsas, K, Kato, S, "Multiprocessor real-time scheduling with a few migrating tasks", 34th IEEE Real-Time Systems Symposium (RTSS 2013), IEEE. 3 to 6, Dec, 2013, pp 170-181. Vancouver, Canada.
17. Marinho, J, Nélis, V, Petters, S, Bertogna, M, Davis, R, "Limited Pre-emptive Global Fixed Task Priority", 34th Real-Time Systems Symposium (RTSS 2013), IEEE. 3 to 6, Dec, 2013, pp 182-191. Vancouver, BC, Canada.
18. Michell, S, Moore, B, Pinho, L, "Real-Time Programming on Accelerator Many-Core Processors", ACM SIGAda High Integrity Language Technology Conference (HILT'13), ACM. 10 to 14, Nov, 2013, pp 23-26. Pittsburgh, U.S.A..
19. Tennina, S, Gaddour, O, Royo, F, Koubâa, A, Alves, M, "Monitoring large scale IEEE 802.15.4/ZigBee based Wireless Sensor Networks", 7th European ZigBee Developers' Conference. 6 to 7, Nov, 2013. Munich, Germany.
20. Nélis, V, Yomsi, P, Goossens, J, "Feasibility Intervals for Homogeneous Multicores, Asynchronous Periodic Tasks, and FJP Schedulers", 21st International Conference on Real-Time Networks and Systems (RTNS 2013), ACM New York. 16 to 18, Oct, 2013, pp 277-286. Sophia Antipolis, France.
Best Presentation Award
21. Awan, M, Yomsi, P, Petters, S, "Optimal Procrastination Interval for Constrained Deadline Sporadic Tasks upon Uniprocessors", 21st International Conference on Real-Time Networks and Systems (RTNS 2013), ACM. 16 to 18, Oct, 2013, pp 192-138. Sophia Antipolis, France.
22. Santy, F, Raravi, G, Nelissen, G, Nélis, V, Kumar, P, Goossens, J, Tovar, E, "Two Protocols to Reduce the Criticality Level of Multiprocessor Mixed-Criticality Systems", 21st International Conference on Real-Time Networks and Systems (RTNS'13), ACM. 16 to 18, Oct, 2013, pp 183-192. Sophia Antipolis, France.

23. Nikolic, B, Ali, H, Petters, S, Pinho, L, "Are Virtual Channels the Bottleneck of Priority-Aware Wormhole-Switched NoC-Based Many-Cores?", 21st International Conference on Real-Time Networks and Systems (RTNS 2013), ACM New York. 16 to 18, Oct, 2013, pp 13-22. Sophia Antipolis, France.
24. Sanchez, F, Pinho, L, Alonso, D, Pastor, J, "Desarrollo de aplicaciones con requisitos de criticidad temporal mixta utilizando C-Forge", 4th Spanish Symposium of Real-Time Systems. 17 to 19, Sep, 2013. Madrid, Spain.
25. Berezovskyi, K, Bletsas, K, Petters, S, "Faster Makespan Estimation for GPU Threads on a Single Streaming Multiprocessor", 18th IEEE Conference on Emerging Technology and Factory Automation (ETFA 2013), IEEE. 10 to 13, Sep, 2013, pp 1-8. Cagliari, Italy.
26. Ferreira, L, Albano, M, Pinho, L, "QoS enabled Middleware for Real-time Industrial Control Systems", 18th IEEE International Conference on Emerging Technologies and Factory Automation (ETFA 2013), IEEE. 10 to 13, Sep, 2013. Cagliari, Italy.
27. Albano, M, Pereira, N, Tovar, E, "How many are you (an approach for the smart dust world)?", IEEE 1st International Conference on Cyber-Physical Systems, Networks, and Applications (CPSNA 2013). 19, Aug, 2013, pp 101-105. Taipei, Taiwan.
28. Nikolic, B, Yomsi, P, Petters, S, "Worst-Case Memory Traffic Analysis for Many-Cores using a Limited Migrative Model", 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013), IEEE. 19 to 21, Aug, 2013, pp 42-51. Taipei, Taiwan.
29. Awan, M, Petters, S, "On the Equivalence of Idealised DVFS and Thermally Constrained DPM in Real-Time Systems", 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013). 19 to 21, Aug, 2013. Taipei, Taiwan.
30. Davis, R, Burns, A, Marinho, J, Nélis, V, Petters, S, Bertogna, M, "Global Fixed Priority Scheduling with Deferred Pre-emption", IEEE 19th International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013), IEEE. 19 to 21, Aug, 2013, pp 1-11. Taipei, Taiwan.
Best Paper Award
31. Dasari, D, Nélis, V, Mosse, D, "Timing analysis of PCM Main Memory in Multicore Systems", 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013), IEEE. 19 to 21, Aug, 2013, pp 52-61. Taipei, Taiwan.
32. Ali, H, Pinho, L, Åkesson, B, "Critical-Path-First Based Allocation of Real-Time Streaming Applications on 2D Mesh-Type Multi-Cores", 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013). 19 to 21, Aug, 2013. Taipei, Taiwan.
33. Sousa, P, Souto, P, Tovar, E, Bletsas, K, "The Carousel-EDF Scheduling Algorithm for Multiprocessor Systems", 19th IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (RTCSA 2013), IEEE. 19 to 21, Aug, 2013, pp 12-21. Taipei, Taiwan.
34. Maia, C, Nogueira, L, Pinho, L, Bertogna, M, "Response-Time Analysis of Fork/Join Tasks in Multiprocessor Systems", Work in Progress Session, 25th Euromicro Conference on Real-Time Systems (ECRTS 2013). 9 to 12, Jul, 2013. Paris, France.
35. Noda, C, Prabh, S, Alves, M, Voigt, T, "On Packet Size and Error Correction Optimisations in Low-Power Wireless Networks", 10th Annual IEEE Communications Society Conference on Sensing and Communication in Wireless

Networks (SECON 2013), IEEE. 24 to 27, Jun, 2013, pp 212-220. New Orleans, LA, U.S.A..
36. Vahabi, M, Tovar, E, Albano, M, "A Self-Adaptive Approximate Interpolation Scheme for Dense Sensing", Work in Progress Session, IEEE International Symposium on Industrial Embedded Systems (SIES 2013), IEEE. 19, Jun, 2013, pp 105-109. Porto, Portugal.
37. Maia, C, Nogueira, L, Pinho, L, "Scheduling Parallel Real-Time Tasks using a Fixed-Priority Work-Stealing Algorithm on Multiprocessors", 8th IEEE International Symposium on Industrial Embedded Systems (SIES2013). 19 to 21, Jun, 2013. Porto, Portugal.
38. Dasari, D, Åkesson, B, Nélis, V, Awan, M, Petters, S, "Identifying the Sources of Unpredictability in COTS-based Multicore Systems", 8th IEEE International Symposium on Industrial Embedded Systems (SIES 2013), IEEE. 19 to 21, Jun, 2013, pp 39-48. Porto, Portugal.
39. Garibay-Martínez, R, Ferreira, L, Maia, C, Pinho, L, "Towards Transparent Parallel/Distributed Support for Real-Time Embedded Applications", 8th IEEE International Symposium on Industrial Embedded Systems (SIES 2013), IEEE. 19 to 21, Jun, 2013, Work-In-Progress Session, pp 114-117. Porto, Portugal.
40. Severino, R, Pereira, N, Tovar, E, "Dynamic Cluster Scheduling for Cluster-tree WSNs", 17 to 19, Jun, 2013.
41. Michell, S, Moore, B, Pinho, L, "Tasklettes – a Fine Grained Parallelism for Ada on Multicores", 18th International Conference on Reliable Software Technologies (Ada-Europe 2013). 10 to 14, Jun, 2013, pp 17-34. Berlin, Germany.
42. Chandrasekar, K, Weis, C, Åkesson, B, Wehn, N, Goossens, K, "Towards Variation-Aware System-Level Power Estimation of DRAMs: An Empirical Approach", 50th ACM/EDAC/IEEE Design Automation Conference (DAC 2013), ACM New York. 29, May to 7, Jun, 2013, 23. Austin, U.S.A..
43. Awan, M, Petters, S, "Energy-Aware Partitioning of Tasks onto a Heterogeneous Multi-core Platform", 19th IEEE Real-Time and Embedded Technology and Applications Symposium (RTAS 2013), IEEE. 29, May, 2013, pp 205-214. Philadelphia, PA, U.S.A..
44. Pinho, L, Michell, S, Moore, B, "Ada and Many-core Platforms", 16th International Real-Time Ada Workshop (IRTAW 2013), ACM New York. 17 to 19, Apr, 2013, 33, 2, pp 40-48. York, United Kingdom.
45. Moore, B, Michell, S, Pinho, L, "Parallelism in Ada: General Model and Ravenscar", 16th International Real-Time Ada Workshop (IRTAW 2013), ACM New York. 17 to 19, Apr, 2013, 33, 2, pp 14-32. York, United Kingdom.
46. Albano, M, Ferreira, L, Guilly, T, Ramiro, M, Faria, E, Dueñas, L, Ferreira, R, Gaylard, E, Cubas, D, Roarke, E, Lux, D, Scalari, S, Sørensen, S, Gangolells, M, Pinho, L, Skou, A, "The ENCOURAGE ICT architecture for heterogeneous smart grids", 11, Apr, 2013. IEEE EuroCon 2013, Zagreb, Croatia, 1-4 July 2013.
47. Groesbrink, S, Almeida, L, Sousa, M, Petters, S, "Fair Bandwidth Sharing among Virtual Machines in a Multi-criticality Scope", 5th Workshop on Adaptive and Reconfigurable Embedded Systems (APRES 2013), ACM New York. 8, Apr, 2013, 10, 4, pp 21-24. Philadelphia, U.S.A..
48. Loureiro, J, Pereira, N, Santos, P, Tovar, E, "A Sensing Platform for High Visibility of the Datacenter", 4th International Workshop on Networks of Cooperating Objects for Smart Cities 2013 (CONET/UBICITEC 2013). 8, Apr, 2013. Philadelphia, PA, U.S.A..

49. Kotaba, O, Nowotsch, J, Paulitsch, M, Petters, S, Theiling, H, "Multicore In Real-Time Systems – Temporal Isolation Challenges Due To Shared Resources", 16th Design, Automation & Test in Europe Conference and Exhibition (DATE 2013). 19 to 26, Mar, 2013. Grenoble, France.
50. Goossens, S, Åkesson, B, Goossens, K, "Conservative Open-page Policy for Mixed Time-Criticality Memory Controllers", Design, Automation & Test in Europe Conference & Exhibition (DATE 2013), IEEE. 18 to 22, Mar, 2013, pp 525-530. Grenoble, France.
51. Shah, H, Knoll, A, Åkesson, B, "Bounding SDRAM Interference: Detailed Analysis vs. Latency-Rate Analysis", Design, Automation & Test in Europe Conference & Exhibition (DATE 2013), IEEE. 18 to 22, Mar, 2013, pp 308-313. Grenoble, France.
52. Chandrasekar, K, Weis, C, Åkesson, B, Wehn, N, Goossens, K, "System and Circuit Level Power Modeling of Energy-Efficient 3D-Stacked Wide I/O DRAMs", Design, Automation & Test in Europe Conference & Exhibition (DATE 2013), IEEE. 18 to 22, Mar, 2013, pp 236-241. Grenoble, France.
53. Gomony, M, Åkesson, B, Goossens, K, "Architecture and Optimal Configuration of a Real-Time Multi-Channel Memory Controller", Design, Automation & Test in Europe Conference & Exhibition (DATE 2013), EDA Consortium San Jose. 18 to 22, Mar, 2013, pp 1307-1312. Grenoble, France.
54. Santos-Jr, J, Lima, G, Bletsas, K, "On the Processor Utilisation Bound of the C=D Scheduling Algorithm", Real-time Systems Workshop. 13 to 15, Mar, 2013. York, United Kingdom.
55. Nogueira, L, Pinho, L, Fonseca, J, Maia, C, "On the use of Work-Stealing Strategies in Real-Time Systems", High-performance and Real-time Embedded Systems (HiRES 2013). 23, Jan, 2013. Berlin, Germany.
56. Rodrigues, V, Åkesson, B, Sousa, S, Florido, M, "A Declarative Compositional Timing Analysis for Multicores Using the Latency-Rate Abstraction", 15th International Symposium on Practical Aspects of Declarative Languages (PADL '13), Springer Berlin Heidelberg, Edited: Kostis Sagonas. 21 to 22, Jan, 2013, 7752, pp 43-59. Rome, Italy.

Conference/Workshop Posters/Demos

57. Chrysoulas, C, Ferreira, L, Albano, M, Petersen, P, Stluka, P, Skou, A, "Virtual Market of Energy: A SOA-based Approach", Poster presented in Artemis ITEA Co-summit. 4, Dec, 2013. Stockholm, Sweden.
58. Teixeira, C, Gonçalves, J, Ferreira, L, Garibay-Martínez, R, Albano, M, Pinho, L, "Middlewares for Embedded Systems", Poster presented in 8th IEEE International Symposium on Industrial Embedded Systems (SIES'13). 19 to 21, Jun, 2013. Porto, Portugal.
59. Berezovskyi, K, Bletsas, K, Petters, S, "Timing analysis for applications running on Graphics Processing Units", Poster presented in 8th IEEE International Symposium on Industrial Embedded Systems (SIES'13). 19 to 21, Jun, 2013. Porto, Portugal.
60. Nikolic, B, Dasari, D, Ali, H, Petters, S, Nélis, V, "Workload Mapping and Resource Management in Many-Core Platforms", Poster presented in 8th IEEE International Symposium on Industrial Embedded Systems (SIES'13). 19 to 21, Jun, 2013. Porto, Portugal.

61. Nelissen, G, Raravi, G, Bletsas, K, Nélis, V, Dasari, D, Souto, P, Tovar, E, "Multi-Processor Scheduling: Paradigms and Challenges", Poster presented in 8th IEEE International Symposium on Industrial Embedded Systems (SIES'13). 19 to 21, Jun, 2013. Porto, Portugal.
62. Loureiro, J, Pereira, N, Tovar, E, Pacheco, F, Vahabi, M, "The SmartSkin Project: Densely Instrumented Physical Infrastructures", Poster presented in 8th IEEE International Symposium on Industrial Embedded Systems (SIES'13). 19 to 21, Jun, 2013. Porto, Portugal.
63. Dasari, D, Awan, M, Nélis, V, Petters, S, "Certification Challenges for Mixed Criticality Systems in Multicores", Poster presented in 8th IEEE International Symposium on Industrial Embedded Systems (SIES'13). 19 to 21, Jun, 2013. Porto, Portugal.
64. Gupta, V, Tovar, E, Pereira, N, Pacheco, F, Pinho, L, Rajkumar, R, "From Sensor Networks to Internet of Things: Wireless Sensor Networks as an Infrastructure Technology", Poster presented in 8th IEEE International Symposium on Industrial Embedded Systems (SIES'13). 19 to 21, Jun, 2013. Porto, Portugal.
65. Berezovskyi, K, Bletsas, K, Petters, S, "Timing analysis for applications running on Graphics Processing Units", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Porto, Portugal.
66. Pereira, N, Loureiro, J, Pacheco, F, Severino, R, Saraiva, B, Oliveira, P, Gupta, V, Tovar, E, Yomsi, P, "The SENODS Project: Sustainable ENergy-Optimized Datacenters", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Porto, Portugal.
67. Awan, M, Yomsi, P, Petters, S, "Energy Efficient Embedded Real-Time Systems", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork2013). 18, Jun, 2013. Porto, Portugal.
68. Loureiro, J, Pereira, N, Tovar, E, Pacheco, F, Vahabi, M, "Reducing Aircraft Fuel Consumption with WSAN-based Active Flow Control", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Porto, Portugal.
69. Pereira, N, Loureiro, J, Pacheco, F, Severino, R, Saraiva, B, Oliveira, P, Gupta, V, Tovar, E, "Dense Instrumentation of Datacenters for Energy-Efficient Management", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Porto, Portugal.
70. Gupta, V, Tovar, E, Pereira, N, Rajkumar, R, "From Sensor Networks to Internet of Things: - A Paradigm for Empowering an Infrastructure Technology", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Porto, Portugal.
71. Sousa, P, Bletsas, K, Tovar, E, Souto, P, Pereira, N, "Enhancing the Real-time Capabilities of the Linux Kernel in Multicore Platforms", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Portugal.
72. Bletsas, K, Tovar, E, Souto, P, Pereira, N, Sousa, P, "Enhancing the Real-time Capabilities of the Linux Kernel in Multicore Platforms", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Porto, Portugal.

73. Fotouhi, H, Severino, R, Alves, M, Pereira, N, Tovar, E, Pacheco, F, Sousa, P, "802.15.4 Technology", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Porto, Portugal.
74. Maia, C, Nogueira, L, Fonseca, J, Pinho, L, Barros, A, "Parallelising Real-Time Software", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Porto, Portugal.
75. Pereira, D, Pedro, A, Pinho, L, "Verification of Hard Real-Time Systems", Poster presented in CISTER 1st Industrial Workshop on Real-Time and Embedded Systems (CiWork 2013). 18, Jun, 2013. Porto, Portugal.

Technical Reports

76. Marinho, J, Nélis, V, Petters, S, "Temporal Isolation with Preemption Delay Accounting", 20, Sep, 2013.
77. Awan, M, Yomsi, P, Petters, S, "Optimal Procrastination Interval upon Uniprocessors", 28, Jun, 2013.
78. Awan, M, Petters, S, "Applying Idealised DVFS Algorithms to Thermally Constrained DPM", 5, Jun, 2013.
79. Awan, M, Petters, S, "Energy and Pre-emption Savings through Real-Time Race-To-Halt Algorithms", 30, May, 2013.
80. "SENODs (Sustainable ENergy-Optimized Datacenters): Building a Microscope for the Datacenter", 12, May, 2013.
81. Berezovskyi, K, Bletsas, K, Petters, S, "Fast Makespan Estimation for GPU Threads on a Single Streaming Multiprocessor", 14, Apr, 2013.

People

www.cister.isep.ipp.pt/people

Åkesson, Benny

PhD Eindhoven University of Technology, Netherlands

Research Associate

Benny Åkesson was born in Landskrona, Sweden in 1977. He earned a M.Sc. degree in Computer Science and Engineering at Lund Institute of Technology, Sweden in 2005. In 2010, he received his Ph.D. degree in Electrical Engineering at Eindhoven University of Technology, the Netherlands, on the topic of "Predictable and Composable SoC Memory Controllers". This research was conducted in collaboration with NXP Semiconductors. Prior to joining the CISTER research unit, Dr. Åkesson worked as Postdoctoral Researcher and Assistant Professor at the Eindhoven University of Technology, where he is led the memory research team in the Electronic Systems group at the faculty of Electrical Engineering. His primary research interests include memory controller architectures, real-time resource scheduling, performance modeling, and virtualization. He is the author of a book about memory controllers for real-time embedded systems.

Albano, Michele

PhD University of Pisa, Italy

Research Associate

Michele Albano received his BSc degree in Physics in 2003, and his BSc, MSc and PhD degrees in Computer Science in 2004, 2006 and 2010 respectively, all of them from the University of Pisa, Italy. He was visiting researcher at Universidad de Malaga (Spain) in 2007, at Stony Brook University (New York, USA) in 2009, and before being a researcher he worked as software engineer and wireless technology specialist in private companies in the period 2001-2006, and he founded an SME. In 2006 and 2007 he was involved in EU funded projects SMEPP and XtreemOs, and in the period 2010-2012 he held a post-doctoral researcher position at the Instituto de Telecomunicações (Portugal), He is currently a Research Scientist in the CISTER and has published the book "Data Centric Storage in Wireless Sensor Networks: Advanced Techniques". His main research interests are in the areas of wireless sensor networks, energy saving in wireless communication, and peer-to-peer networks.

Al-Asadi, Amine

Technical Staff, Administrative Support

Amine Al-Asadi joined the Cister Research Unit in September 2011. She is part of our technical support staff and assists the group in organizational matters as well as administrative work.

Ali, Kiran

MSc Student

Kiran Ali got her first degree in Computer Science from Gomal University, Dera Ismail Khan, Pakistan. Currently, she is pursuing a Master's in Computer Science with specialization in Parallel and Distributed Systems from University of Porto, Portugal. Her area of interest is Parallel and Distributed Embedded Systems.

Ali, Hazem

PhD Student

Hazem completed his MSc in Embedded and Intelligent Systems at the School of Information Science of the Halmstad University, Sweden, September 2010. He is currently doing his PhD at CISTER in the area of real-time languages.

Alkhawaja, Abdel Rahman

PhD Student

Abdel Rahman received his bachelor degree in Computer Engineering form University of Jordan in 2006 and completed his master in Computer Network Engineering in Halmstad University, Sweden, 2011. He has previously worked in network operation center.
His research interests are wireless sensor networks, mobile communication system and networking. Currently, he is doing his PhD at CISTER Research Unit.

Almeida, Inês

Administrative Assistant

Inês Almeida used to live in Brussels where she worked as a professional contemporary performer. Four years ago she came back to her origins and got her degree in Administrative Assistance and Translation from the Administration and Accountancy School of the Polytechnic Institute of Porto. Currently, she is pursuing a Master's in Innovation and Technological Entrepreneurship at the Faculty of Engineering of the University of Porto, Portugal.

Almeida, Sandra

Management Support

Sandra Almeida joined the group in 2002. She is the Financial & Administrative Manager. She got a degree in Management Assessorship, from the Polytechnic Institute of Porto, School of Accounting and Administration.

Alves, Mário

PhD University of Porto, Portugal

Professor, Research Associate

Mário Alves was born in 1968 and has a Degree (1991), a MSc (1995) and a PhD (2003) in Electrical and Computer Engineering at the University of Porto, Portugal. He is a Professor in ECE at the Polytechnic Institute of Porto (ISEP/IPP) and a Research Associate and Wireless Sensor Networks (WSNs) research line leader at CISTER. He has been actively participating in the organization of several international conferences and workshops (e.g. EWSN, ECRTS, IEEE WFCS, CONET). His personal research interests are mainly devoted to supporting quality-of-service (QoS) in large-scale and dense WSNs, mainly based on standard and COTS technology. He is currently involved in several national and international projects and networks of excellence. The WSN team at CISTER has been attaining many important achievements and international visibility, such as 1) deploying the largest WSN test-bed in Europe so far (300+ nodes, under the EMMON project); 2) scoring over 115000 visits and 6000 downloads of the open-ZB toolset; and 3) being founding members of and active contributors to the TinyOS 15.4 and ZigBee Working Groups.

Awan. Muhammad Ali

PhD Student

Muhammad Ali Awan did his master's Degree from Royal Institute of Technology(KTH) Sweden in System on Chip Design with a focus on Digital System Design and Embedded Systems. He worked as Lecturer in National University of Science and Technology Pakistan. He also worked as a researcher in IMEC, Belgium for two years. His research focus was on High Level Memory Management. Currently he started his PhD in Cister and participating in a research on "Real-Time Power Management on Partitioned Multicores".

Baldovin, Andrea

Visiting PhD Student

Andrea Baldovin is a PhD student in Computer Science at the University of Padua. He received his Bachelor's and Master's Degree from the same institution, where he has been involved in the EU-FP6 SPADE project and in the EU-FP7 PROARTIS project. His research interests include Worst-Case Execution Time (WCET) Analysis of hard real-time systems, with particular attention to time-composable architectures and real-time operating systems.

Barros, Cristiana

Administrative Assistant

Cristiana Barros was born and raised in the town of Chaves. In 2003 she moved to Oporto to study Communication, Public Relations, Advertising and Marketing; from an early age she developed an interest in the audiovisual area, having her first audiovisual experience as Second Assistant Director in 2006, in the short film "Área Protegida" by José Miguel Moreira.
She has worked along with Paulo Calheiros as her assistent making her first steps into photography. Currently she is attending a degree in Audiovisual and Multimedia Communication and working as a freelancer photographer.

Barros, António

Lecturer, PhD Student

António Manuel de Sousa Barros was born in 1974 and has a 5 year degree (1997) and a master degree in Electrical and Computer Engineering at the Universtity of Porto.Since 2001 he has been a teacher assistant at the Department of Computer Engineering. He was researcher at the Biomedical Engineering Institute (University of Porto) from 1998 to 2001. He also worked as freelancer in the fields of electronics and computer programming. Since January 2005 he is also with the CISTER.His interests are in real-time telecommunication systems and reliable software.

Berezovskyi, Kostiantyn

PhD Student

Kostiantyn Berezovskyi holds M.Sc. degree from Taras Shevchenko National University of Kyiv. At university he paid great attention to software development and have gathered experience in parallel programming. Now he is a PhD student at CISTER. His interests are related to the schedulability analysis of general purpose graphics processor units.

Bletsas, Konstantinos

PhD University of York, United Kingdom

Research Associate

Konstantinos Bletsas (born in 1978 in Greece) has a Degree in Electronic and Computer Engineering (2002) from the Technical University of Crete (Chania, Greece) and a PhD in Computer Science (2007) from the University of York (UK). His PhD was about the response time analysis of hard real-time systems with application-specific co-processors. He joined the group in 2007 to do research on multiprocessor scheduling algorithms.

Burmyakov, Artem

PhD Student

Artem Burmyakov received a masters' degree in Computer Sciences from Moscow Engineering and Physics Institute. He worked as a software engineer within CERN for more than 4 years, participating in the LHC GCS and the UAB projects. Nowdays he is a doctoral student within CISTER. His professional interests are related to the development of control, real-time and distributed systems.

Carvalho, Paulo

Technical Staff

Paulo David Peixoto de Carvalho (born in 1993 in Miragaia, Porto) graduated in Electronic, Automation and Computers in Escola Profissional de Tecnologia e Electrónica (ESTEL). At its Professional Aptitude Test (PAP) he presented a Home
Automation controlled by programming in Visual Basic 2010 and CX-Programmer, working from an automaton CP1L. Since finishing the course (2011) he had the opportunity to work in the field of automotive painting and as a telecommunications sales technician.
He is currently working at CISTER/INESC-TEC providing support for the operation and maintenance of equipment and infrastructure.

Castanho, Francisco

MSc Student

Francisco Castanho was born in 1989 and has a bachelor's degree(2012) in Informatics engineering by the School of Engineering, Polytechnic Institute of Oporto. Currently he is developing his Master's Thesis at CISTER. His main interests are real-time systems, multi-processor scheduling algorithms, and safety-systems.

Chrysoulas, Christos

PhD University of Patras, Greece

Research Associate

Christos Chrysoulas received his PhD in Electrical & Computer Engineering from the Electrical & Computer Engineering Dept., University of Patras, Greece in 2009. He received his Diploma in Electrical & Computer Engineering from the Electrical & Computer Engineering Dept., University of Patras, Greece in 2003. Since then he is working as an Adjunct Professor, in the Technological Educational Institute of Patras, Hellas. His research interests include Computer Networks, High Performance Communication Subsystems Architecture and Implementation, Wireless Networks, New Generation Networks Architectures, Resource Management and Dynamic Service Deployment in New Generation Networks and Communication Networks, Grid Architecture, Semantics.

Clement, Gareth

Science & Technology Management

Gareth Clement completed his undergraduate degree in Chemistry at the university of Teesside in the UK (1996). While working in Operations Management in the UK he decided to further his education and studied for his MBA at Thames Valley University (now University of West London) in 2005. After completing his studies he was invited to lecture by the Business Management School at the university. Gareth went on to complete his Project Management Professional Qualification from the Project Management Institute (www.pmi.org). In 2009 was invited to join Critical Software being responsible for the I&K (Innovation & Knowledge) dept focusing on the R&D for the organisation alongside being the Project Manager on some of the research projects.

Dasari, Dakshina

PhD Student

Dakshina Dasari was born in 1980 in India. She has a Bachelors Degree from Karnataka University Dharwad and finished her Masters in 2004 from National Institute of Technology, Surathkal (NITK), India. She has five years of working experience - 3 yrs at Sun Microsystems and 2 yrs at Citrix Pvt Ltd as Software Engineer. She has previously worked in the area of Networking.

Duarte, Roberto

Undergrad Student

Roberto Daniel Alves Duarte was born on 1988. He is in the third year of a Bachelor degree in Informatics engineering by the School of Engineering, Polytechnic Institute of Oporto. Currently he is developing his bachelor's internship at CISTER. His main interests are Adaptive RT Systems, RT Software and Multi-core Systems.

Dumez, Thomas

Undergrad Student

Thomas Dumez was born in Liège, Belgium, in 1986. He is in the third year of a Bachelor degree in Industrial Computer Science at "Haute Ecole de la Province de Liège (Belgium)". To complete his studies, he decided to do an Erasmus in Porto and join CISTER Research Unit where he is studying the topic "Implementation of a work-stealing scheduler in a real-time operating system".
During his curriculum, he has studied several subjects from which the following are highlighted: real-time operating systems, real-time programming (POSIX 1003.1b), embedded systems, robotics and microprocessor architectures.

Easwaran, Arvind

PhD University of Pennsylvania, U.S.A.

Research Associate

Arvind Easwaran was born in Mumbai (formerly Bombay), India, in 1979. In 2001 he graduated with a Bachelor of Engineering (BE) in Computer Engineering from Mumbai University, India. After that he had a brief stint first at the Indian Institute of Technology (IIT), Bombay, as a Project Engineer with Prof. Subramani Arunkumar, and then at Infosys Technologies Ltd. as a Software Engineer. In 2005 he was awarded the Master of Science in Engineering (MSE) degree, and in 2008 he was awarded the Doctor of Philosophy (PhD) degree, both in Computer and Information Science from the University of Pennsylvania, USA. His academic advisors were Prof. Insup Lee and Prof. Oleg Sokolsky. During PhD studies, he also had a brief stint at Honeywell, Advanced Technology, as a research intern. Since January 2009, he has been working at CISTER as a research scientist in the area of real-time scheduling theory.

Ferreira, Luis Lino

PhD University of Porto, Portugal

Professor, Research Associate

Luis Lino Ferreira was born in 1971 and has a MSc (1997) and a PhD (2005) in Electrical and Computer Engineering at the University of Porto. Since 1996 he works as a professor at the Department of Computer Engineering, School of Engineering of the Polytechnic Institute of Porto. He was a researcher at the Systems and Robotics Institute, Industrial Automation Group (University of Porto), from 1994 to 1996, in the area of Real-Time Control Systems. Since 1997 he is a member of the IPP-HURRAY research group, where he is currently working on Wireless and mobile networks.

Fonseca, José

PhD Student

José Carlos Fonseca was born in 1987, in Porto, Portugal. He holds a BSc (2010) and a MSc (2012) both in Computer Engineering from the School of Engineering of the Polytechnic Institute of Porto (ISEP). Currently, José is pursuing a PhD in Electrical and Computer Engineering at the University of Porto. Since he joined CISTER Research Unit in February 2012, his main research interests are in real-time operating systems and scheduling theory for multi- and many-core platforms.

Fotouhi, Hossein

PhD Student

Hossein Fotouhi received his degree on Electrical Electronics Engineering in 2004 and worked afterwards about three years in Iran in different places such as University of Guilan and Telecommunication Center as a network engineer. He obtained his Master of Science in Communication Network Engineering in 2009 from University Putra Malaysia. His MSc thesis was on "optimizing energy consumption in MAC layer for Wireless Sensor Networks"Currently, he is doing his PhD research in CISTER Research Unit since July 2009. His research interests are wireless sensor networks, mobility management, handoff mechanism and fuzzy logic theory.

Garibay-Martínez, Ricardo

PhD Student

Ricardo Garibay-Martínez was born on 1984 in Morelia, Mexico. Ricardo received his Bachelors Degree from Morelia Institute of Technology (ITM) in 2007 and finished his Master of Science in Computer Science from Centre for Scientific Research and Higher Education of Ensenada (CICESE), Mexico. He has experience working as a lecturer and as a researcher for PEMEX Petroleum Company. Since 2007, he has been working in the area of Adaptive Resource Management in Distributed Dynamic Real-Time Systems.Currently, he is working as a researcher and PhD student in CISTER/IPP-HURRAY Research unit. His current research interests are Adaptive RT Systems, RT Software and Multi-core Systems.

Gaur, Shashank

PhD Student

Shahsank Gaur is a recent graduate from ECE Paris in Embedded System. His research interest are Wireless Sensor networks, Software Defined Radio, etc. He has extensively worked on various industrial and research projects in past with organizations such as GNURadio, EADS, Infineon Technologies, Ansaldo STS(Finmeccanica Group), Aldebaran Robotics, etc.Before graduating from ECE Paris, he completed undergraduate studies in Electronics and Communications from BKBIET, Pilani, India in 2011.

Gonçalves, Joel

Junior Researcher

Joel Gonçalves graduated in Informatics Engineering at the School of Engineering, Polytechnic Institute of Porto, in 2010. In 2012, he got his MSc in Informatics Engineering and Computation at the Faculty of Engineering, University of Porto. His main research interests are software architecture, distributed systems, real-time systems and simulation. Joel worked in research centers in Portugal (CISTER/ISEP and LIACC/FEUP) and Germany (LFE/TUM) where he covered many subjects from the mentioned research areas. He has published several papers in national and international conferences.Currently he is enrolled in the PhD program in Informatics Engineering at Faculty of Informatics Engineering, University of Porto.

Gupta, Vikram

PhD Student

Vikram Gupta is a PhD candidate in Electrical and Computer Engineering in the Carnegie Mellon University (CMU) - Portugal joint program beginning August 2008 and is supervised by Prof. Raj Rajkumar (ECE-CMU) and Prof. Eduardo Tovar (ISEP-IPP). His current research includes developing clock synchronization methods for Wireless Sensor Networks. Before joining PhD program, he was working as a research associate at Indian Institute of Technology (I.I.T.) Delhi, India, where he focussed on Performance Assessment and Interoperability of WiMAX (802.16) on a Campus based Test Bed. He received his degree of Bachelor of Technology from National Institute of Technology (V.N.I.T.) Nagpur India in May 2007.

Ijaz, Hamza

Junior Researcher

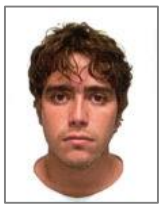
Hamza Ijaz has a master's in Design and Implementation of ICT Products and Systems from Royal Institute of Technology(KTH) Sweden and a bachelor's in Electrical and Computer Engineering from Center for Advanced Studies in Engineering(CASE) Pakistan. Hamza has worked in research and development projects addressing various aspects of embedded and electronics systems.His main areas of interest are embedded systems, sensor based systems, high speed digital design and machine vision.

Koubâa, Anis

PhD Nat. Polytechnic Institute/INPL, France

Professor, Research Associate

Anis KOUBÂA was born in 1977 in Tunisia and has an Engineering Degree in Telecommunications (2000) from Sup'Com (Tunisia), a Master Degree in Computer Science (2001) from University of Nancy I (France), and a PhD in Computer Science (2004) from National Polytechnic Institute (INPL). His PhD work addressed the definition and analysis of graceful degradation of real-time quality of service in guaranteed-rate Networks using (m,k)-firm model. From March 2005, he is involved in a post-doc project on Real-Time Communication in Wireless Sensor Networks at CISTER research group. His main research activities focus on real-time, quality of service and wireless sensor networks. His Post-Doctoral work in CISTER is focused on Wireless Sensor Networks with an emphasis on real-time aspects.



Loureiro, João

PhD Student

João Loureiro holds a degree in Mechatronic Engineer since 2009 from Pontifícia Universidade Católica de Minas Gerais, Brazil. He has worked in research and development of embedded systems, both inside industry and university. His research interests are in Real Time Embedded Systems, Cyber-Physical Systems and Sensor Networks. Currently his research is includes the development of a network architecture for extreme dense sensing for active flow control. João Loureiro is a PhD candidate in Electrical and Computer Engineering in FEUP and researcher at the CISTER Research Unit.

Maia, Cláudio

PhD Student

Cláudio Maia, born in 1980, holds a degree (2007) in Computer Science Engineering at the Polytechnic Institute of Oporto.
From 2006 to 2009, he was a researcher and software engineer at Critical Software S.A. During that time, his main areas
of research were mobile and wireless communication systems and manufacturing systems.
Since October 2009, he is a Researcher in the CISTER Research Unit, involved in the CooperatES project.His main research interests are in the fields of Dynamic Distributed Real-time Systems, Operating Systems and Mobile and Wireless Communication Systems.

Marau, Ricardo

PhD University of Aveiro, Portugal

Research Associate

Ricardo Marau is a Research Fellow at CISTER - Research Center in Real-Time and Embedded Computing Systems. He graduated in Electronics and Telecommunications Engineering in 2004 and received his PhD degree in Computer Engineering from the University of Aveiro, in 2009. He visited the University of Cantabria, Spain, in 2005, the Polytechnic University of Valencia, Spain, in 2008, the Carnegie Mellon University in Pittsburgh, USA, in 2008, and the University Carlos III, Spain, in 2010. During the period of 2009-2012 he has been a research fellow at the Electrical and Computer Engineering Department of the University of Porto, being involved in the project iLAND (EU ARTEMIS JU) as technical manager and work-package leader. His research interests are on Switched Ethernet Real-time, scheduling and communication middlewares.

Marín Carrión, Ismael

PhD University of Castilla-La Mancha, Spain

Research Associate

Ismael Marín Carrión received a PhD and MRes in Advanced Computer Science from the University of Castilla-La Mancha (Spain) in 2010 and 2006 respectively, a ME in Computer Science in 2003 and a BE in Computer Systems in 2001, also from the University of Castilla-La Mancha. Ismael has held different positions in both university and industry, including several research visits. In 2013, Ismael has joined to CISTER as a postdoc researcher. The main research interests are concerned to grid computing, parallel computing and distributed systems.

Marinho, José

PhD Student

José Marinho holds an MSc degree on Electrical Engineering from the University of Coimbra (2008). He has previously worked at Instituto de Telecomunicações (Coimbra, Image Processing Lab) during his master thesis (LDPC decoding on the CELL/BE marked 20/20). Later José moved onto the Instituto de Sistemas e Robótica Coimbra (Mobile Robotics Lab) where he worked for a year period as a fresh graduate researching on and implementing bayesian inference mechanisms. José has a big interest on the embedded computing panorama. Being on the final leg of his PhD José is currently looking for opportunities to extend his knowledge in the fields of embedded operating systems and related hardware within the real-time context or other affine research fields.

Mekki, Maher

Undergrad Student

Maher was born in 1988 in Tunisia and he is a third year engineering student in the high school of communication Tunis (Sup'com). Currently, Maher is a trainee at Cister-Research Unit within his graduation internship. His interests are in telecommunication engineering, computer network and programming.

Moreira, Daniel

Undergrad Student

Daniel Moreira was born in 1987. Received a degree in Electrical and Computer Engineering (2010) from the Polytechnic Institute of Porto - School of Engineering. He is currently completing his MSc in Telecommunications and has been collaborating with CISTER in the field of Wireless Sensor Networks with an emphasis in mobility management and handoff mechanisms to complete his thesis on this subject.

Moreno, Maria

PhD Intern

Maria Ángeles Serna received her BSc degree in Computer Science in 2008 and her M.Sc. degree in Advanced Computer Technologies in 2010, both from the University of Castilla-La Mancha. She is also a PhD student and her research interests include collaborative processing of environmental information in wireless sensor networks, including data dissemination techniques, phenomena monitoring, modeling and simulation.

Nélis, Vincent

PhD Université Libre de Bruxelles, Belgium

Research Associate

Vincent Nélis was born in Brussels, Belgium, in 1984. In 2006 he received his master's degree in Computer Science at U.L.B. (Université Libre de Bruxelles), Belgium. During the same year, his Master's Thesis was awarded by a prestigious belgian prize: "Solvay Awards 2006". From 2006 to 2010, Vincent worked in two successful departments of U.L.B.: the "Scheduling Group" and the BEAMS (Bio-, Electro- And Mechanical Systems). In 2010, he earned his Ph.D. degree in Computer Science at U.L.B under the supervision of Prof. Joël Goossens. He is currently working at CISTER/IPP-HURRAY as a research scientist in the area of real-time scheduling theory. His research interests include: cyber-physical systems, real-time scheduling, real-time communication.

Nelissen, Geoffrey

PhD Université Libre de Bruxelles

Research Associate

Geoffrey Nelissen was born in Brussels, Belgium in 1985. He earned his MSc degree in Electrical Engineering at Université Libre de Bruxelles (ULB), Belgium in 2008. Then, he worked during four years as a PhD student in the PARTS research unit of ULB. In 2012, he received his PhD degree under the supervision of Professors Joël Goossens and Dragomir Milojevic, on the topic "Efficient Optimal Multiprocessor Scheduling Algorithms for Real-Time Systems". He is currently working at CISTER as a researcher scientist in the area of multiprocessor real-time scheduling theory. His research interests include real-time scheduling theory, real-time operating systems and multi-processors/multi-cores architectures.

Nikolic, Borislav

PhD Student

Borislav graduated at the Faculty of Electrical Engineering in Belgrade with major in Computer Science in 2007. He spent almost two years in industry developing large-scale enterprise applications. Currently, Borislav is doing his PhD at CISTER/IPP-HURRAY Research unit. He is amateur road cyclist and big fan of FC Red Star Belgrade. His research interests include real time and embedded systems, distributed and parallel computing, gossip protocols, ORMs and software architecture and design.

Noda, Claro

PhD Student

Claro Noda graduated in Physics from University of Havana, Cuba in 1996. He worked in Scientific Instrumentation at the Superconductivity Laboratory, IMRE (1996-2001) where he completed his Master in Physical Sciences in 2000 and later continued research activities at the "Henri Poincaré" Complex Systems Group. He has also taught at the General Physics Department in the Faculty of Physics in Havana (2005-2008). Currently he's a MAP-Tele PhD student at University of Minho and a researcher at CISTER/ISEP, Portugal.

Nogueira, Luis Miguel

PhD University of Porto, Portugal

Professor, Research Associate

Luís Nogueira got his BSc in Computer Engenineering at the School of Engineering, Polytechnic Institute of Porto, in 2000. In 2002, got his MSc and in 2009 his PhD in Informatics (Systems and Networks) at the Faculty of Science, Univeristy of Porto. Since 2001 he is teaching assistant at the Department of Computer Engineering of the School of Engineering of the Polytechnic Institute of Porto. From 2000 to 2003 he was a researcher at NIAD&R (Distributed Artificial Intelligence & Robotics Group) of LIACC (Artificial Intelligence and Computer Science Lab), University of Porto. Now, his current research interests are in the fields of Dynamic Distributed Real-time Systems, Quality of Service and Ad-hoc Networks.

Pacheco, Filipe

PhD University of Porto, Portugal

Research Center Adjunct Director

Professor, Research Associate

Filipe de Faria Pacheco Paulo (born Filipe de Faria Pacheco in 1971) has a degree (1994), MSc (1997) and PhD (2009) in Electrical and Computer Engineering at the University of Porto. Since 1996 he is a teaching assistant at the Department of Computer Engineering, - School of Engineering of the Polytechnic Institute of Porto. He was researcher at the Systems and Robotics Institute, Industrial Automation Group (University of Porto), from 1994 to 1996, in the area of User Interfaces. He is currently working in Multimedia and Real-Time networks projects.

Pasdeloup, Bastien

Undergrad Student

Bastien Pasdeloup was born in 1988 in Brest, France. He started his studies in computer science in 2008 when he entered an Associate Degree in Brest. After a year at ENIB, a French engineering school, he decided to dedicate himself to research, and applied to ENS Cachan, Brittany extension, where he is still studying.
His interests are very varied, and cover many fields of computer science, from system to high level programming languages, also including fields such as security and machine learning.
He will stay in Porto for his internship from the 20th of May to the end of August.

Pedro, André

PhD Student

André Pedro was born in Covilhã, Portugal, in 1987. In 2009 he received his degree in Computer science engineering at Universidade da Beira Interior, Covilhã. In 2011 he has concluded the Master's degree in Computer science engineering at Universidade do Minho, Braga with thesis "Learning and testing Stochastic discrete event systems". Now, he begin his Phd study where must be highlighted the Ada contracts for verification of real-time systems. His research interests include: discrete event systems, real-time scheduling, and model-checking.

Pereira, David

PhD MAPi, Portugal

Research Associate

David Pereira was born in Porto, Portugal, in 1980. In 2003 he received his degree in Computer Science at University of Porto. In 2007 he finished his Master's degree in Computer Science also in University of Porto, in the areas of formal logics for specifying and reasoning about intelligent agents. He has a PhD in Computer Science, in the MAP-i PhD program, organized by the Universities of Minho, of Porto and of Aveiro. His research is focused in the mechanization of Kleene algebra and Kleene algebra with tests in the Coq theorem prover (see http://coq.inria.fr/). He also mechanized a deductive proof system for dealing with the partial correctness of parallel programs, under the spirit of Rely/Guarantee thinking. Besides being a happy Coq user and adept of formal program verification, David is keen to apply is formal methods background into the realm of programming languages for real-time programs, namely the well-know and powerful Ada.

Pereira, Miguel

Technical Staff

Nuno Miguel Pereira was born in 1972 at Lisbon, worked from 1996 to 1998 at Efacec in manufacture of Power transformers. Since then he turned to computers and audiovisual equipment at end-user market, business market and educational market.
His interests are home cinema, new technologies and renewable energies.

Pereira, Nuno

PhD University of Minho, Portugal

Professor, Research Associate

Nuno Pereira received a degree in computer engineering from the School of Engineering, Polytechnic Institute of Porto, Porto, Portugal, a M.Sc. and Ph.D. degrees from the University of Minho, Braga, Portugal, in 2002 and 2005 and 2010 respectively. He is a researcher at CISTER, a top-ranked research unit of the Portuguese research system since 2001. He started his research work dedicated to traffic scheduling combining multimedia and industrial communication protocols, and also analyzed the timing behavior of several industrial communication protocols. More recently, Nuno developed novel medium access control protocols for wireless networks and explored efficient ways to obtain aggregated quantities in large scale, dense wireless networks.

Petters, Stefan M.

PhD Technical University Munich, Germany

Research Centre Vice-Director

Research Associate

My research interests include real time and embedded systems in general and more specifically system energy management, mixed-criticality systems, adaptive real-time systems, (probabilistic) worst case execution time (WCET) analysis, and (probabilistic) schedulability analysis.

Pinho, Luis Miguel

PhD University of Porto, Portugal

Research Centre Vice-Director

Professor, Research Associate

Luis Miguel Pinho has a MSc (1997) and a PhD (2001) in Electrical and Computer Engineering at the University of Porto. He is Coordinator Professor at the Department of Computer Engineering - School of Engineering of the Polytechnic Institute of Porto, and Vice-Director and Research Associate at the CISTER research unit, where he currently leads the real-time software research line. His main research interest is on the software infrastructure for real-time embedded systems, in particular languages and operating systems. He is especially interested in Ada, the best language for real-time embedded systems. Miguel is a member of ISO/IEC JTC1/SC22/WG9 and board member of Ada-Europe. He served as General Chair and Program Co-Chair of the Ada-Europe 2006 conference, was a Keynote Speaker at RTCSA 2010 and Program Co-Chair of Ada-Europe 2012. He is Editor-in-Chief of the Ada User Journal, and a member of the HiPEAC network of excellence.

Prabh, Shashi

PhD University of Virginia, U.S.A.

Research Associate

Shashi Prabh received M.S. and Ph.D. in Computer Science from New York University in 2001 and the University of Virginia in 2007, respectively. He joined the Real-Time Computing Systems Research Center (CISTER) of the School of Engineering (ISEP), Polytechnic Institute of Porto (IPP) as Research Associate in 2007. The areas of his research are modeling, analysis and quality of service provisioning in wireless networks. He has contributed to the research on real-time communications in wireless ad-hoc and sensor networks.

R., Raghu

PhD IIT Bombay, India

Research Associate

Raghu received his PhD from IIT Bombay in 2009. He was at Motorola Labs Bangalore, since 2008, working on protocol analysis in data wireless networks. After leaving the labs, he started a firm consulting in wireless systems design and development. He is currently at CISTER, ISEP, Porto. His areas of interest include architecting and building sensor network systems and especially, developing low cost solutions using open standards and COTS.

Raravi, Gurulingesh

PhD Student

Gurulingesh Raravi finished his Masters Degree at IIT Bombay in 2005. He has three years of working experience. Currently, he is pursuing PhD in the area of Real-Time Scheduling on Heterogeneous Multiprocessor Platform.

Ribeiro, André

IT Support

André Ribeiro was born in 1991 in S. João da Madeira. In 2009, André finished his high school degree specialised in Information System's Management and Programming, and in 2012 his Bachelor in Informatics Engineering/Computer Science. Currently, André is enrolled at ISEP, in the Master Programme in Informatics Engineering/Computer Science.

Sanchez, Francisco

PhD Student

Francisco Sánchez was born on 1985 in Santo Domingo, Dominican Republic. He received his Bachelor's Degree in Electronics and Communications Engineering from the Instituto Tecnológico de Santo Domingo (INTEC) in 2009 and M.Sc. Degree on Information and Communication Technology from Technical University of Cartagena in 2010.
Currently, Francisco is pursuing a PhD in Information and Communication Technology at the Technical University of Cartagena. His main research interests are: Model Driven Engineering (MDE), Software Design Patterns and Real Time Systems.

Santos, Pedro

Technical Staff

Pedro Santos was born in 1994 in Porto, and is currently enrolled in the 2nd year of the FEUP's course, in Electrical and Computer Engineering, at the University of Porto. His main interests are in the fields of Wireless Sensor Networks, Real-time Systems, Programming, Artificial Intelligence, Automation and Electronics Systems.

Saraiva, Bruno

MSc Student

Bruno Saraiva, born in 1987, holds a degree (2010) in Computer Science Engenineering at the School of Engineering, Polytechnic Institute of Oporto. Currently he is developing his Master´s Thesis at CISTER Research Unit, involved in the SENODS project. His main interests are in the field of Networking, Multi-Agent Systems and Mobile.

Severino, Ricardo

Lecturer, PhD Student

Ricardo Severino was born in 1982 and has a Degree (2006), and a MSc (2008) in Electrical and Computer Engineering at the Polytechnic Institute of Porto – School of Engineering (ISEP/IPP). Since 2006, he has been working in the area of Wireless Sensor Networks, namely on improving quality-of-service (QoS) in WSNs by using standard and commercial-off-the-shelf (COTS) technology, at CISTER. In this line, he has been actively participating in the ART-WiSe and Open-ZB research frameworks, as well as in international projects such as ArtistDesign, CONET, and EMMON. He is also a founding member and contributor of the 15.4 and ZigBee TinyOS Working Groups. Recently, his MSc Thesis work was awarded with the EWSN'09 Best MSc Thesis Award at the prestigious European Conference on Wireless Sensor Networks (EWSN'09).

Silva, Eduardo

Technical Staff

Eduardo Silva was born in 1975 at Porto, Portugal, from 1994 to 1998 he attended Advertising at Universidade Fernando Pessoa, from 1999 to 2013 worked as computer technician in the final-costumer market.
His main interests are Information Technologies and Astronomy.
He dreams that one day he may have a quantum computer at his desk.

Soares, Bruno

Undergrad Student

Bruno Soares, born in 1989, is a third-year student in Computer Engineering at the School of Engineering of the Polytechnic Institute of Porto. He's currently working on a code mobility library for Android operating systems. His main interests are mobile programming, software engineering, and networks.

Sotomaior, Tomás

Undergrad Student

Tomás Sotomaior was born in 1990 in S. Mamdede Infesta. In 2008, Tomás finished his High School Technological Course in informatics. Currently, he is enrolled in the 3rd year of the ISEP's course in Computer Engineering at the School of Engineering, Polytechnic Institute of Oporto, and is doing is internship at CISTER Research Group, working on distributed parallel programming techniques.

Sousa, Paulo Gandra de

PhD University of Minho, Portugal

Professor, Research Associate

Paulo Gandra de Sousa is a Professor of Informatics at Instituto Politécnico do Porto (Polytechnic Institute of Porto, Portugal) - ISEP/IPP since 1996. He graduated in 1995 from ISEP-IPP; in 1998, he concluded a post-graduation on "Distributed Systems, Computer Architectures and Computer Communications" at Universidade do Minho (University of Minho, Portugal), and achieved his PhD in 2002 (also from Universidade do Minho). He worked for 3 years as an application developer for a Portuguese software house in the field of electronic archive, database retrievals and component development. Prior to CISTER he was a member of the R&D Group on Knowledge Engineering and Decision Support (GECAD, ISEP/IPP) and the technical contact point for the ISEP/IPP node of AgentLink – European Network of Excellence in Agent Based computing. He is one of the founders of the Portuguese chapter of the International Association of Software Architects (IASA). His main research interests are Distributed (Intelligent) Systems, Large Scale Systems, and Enterprise Application Architectures.

Sousa, Paulo Baltarejo

PhD University of Porto, Portugal

Lecturer, Research Associate

Paulo Baltarejo Sousa received a degree in computer engineering from the School of Engineering, Polytechnic Institute of Porto, in 2003. In 2007, he received an MSc in Electrical and Computer Engineering from Technical Institute, Technical University of Lisbon. In 2013, he received a PhD in Informatics Engineering from Faculty of Engineering, University of Porto. Since 2003 he is teaching assistant at the Department of Computer Engineering of the School of Engineering of the Polytechnic Institute of Porto and also research at CISTER. Now, his current research interests are in the field of real-time scheduling algorithms for multiprocessor systems with special focus on implementations in operating systems.

Teixeira, José

Undergrad Student

José was born in 1991 in Porto. José has a high school degree specialized in Information System's Management and Programming. Currently, he is enrolled in the 3rd year of the ISEP's course in Computer Engineering at the School of Engineering, Polytechnic Institute of Oporto, and is doing is internship at CISTER Research Group, working on code offloading for mobile systems.

Teixeira, César

MSc Student

César Teixeira, born in 1987, holds a degree (2010) in Computer Science Engenineering at the School of Engineering, Polytechnic Institute of Oporto. Currently he is involded in the ENCOURAGE project.His main interests are in the field of Networking, Mobile, Multi-Agent Systems and Web development.

Tennina, Stefano

PhD University of L'Aquila, Italy

Research Associate

Stefano Tennina was born in L'Aquila, Italy, in 1978. He received the Laurea degree (cum laude) in Electronic Engineering from the University of L'Aquila, Italy, in 2003 and the Ph.D. degree in Electrical and Information Engineering from the same Institution in 2007. Since August 2002, he has been with the Department of Electrical and Information Engineering and the Centre of Excellence in Research DEWS, holding the position of post-doctoral researcher. He is currently a Research Scientist in the CISTER Research group, involved in the EMMON project of the ARTEMISIA 7th European Framework. His main research interests are in the area of communication protocol design, and wireless communication systems, with particular emphasis on applied analysis and experimentation on physical networks testbeds. His current research activity is mainly focused on fully distributed positioning algorithms, and source coding.

Thamri, Meriam

Undergrad Student

Meriam Thamri was born in 1988 in Tunisia. Currently, she is a third year engineering student at the Higher School of Communication of Tunis (Sup'Com). For her graduation project, she was accepted as a trainee for a 6 month internship in the CISTER Research Unit. Her work will be focused on wireless sensor networks and the handoff process. Her interests are mainly in the areas of information and communication technologies, mathematics and programming.

Tovar, Eduardo

PhD University of Porto, Portugal

Research Centre Director

Professor, Research Associate

Eduardo Tovar is the head of CISTER Research Center. He was born in 1967 and has received the Licentiate, MSc and PhD degrees in electrical and computer engineering from the University of Porto, Porto, Portugal, in 1990, 1995 and 1999, respectively. Currently he his Professor of Industrial Computer Engineering in the Computer Engineering Department at the Polytechnic Institute of Porto (ISEP-IPP), where he is also engaged in research on real-time distributed systems, wireless sensor networks, multiprocessor systems, cyber-physical systems and industrial communication systems. He heads the CISTER Research Center, a top ranked ("Excellent") unit of the FCT Portuguese network of research units. Since 1991 he authored or co-authored more than 100 scientific and technical papers in the area of real-time computing systems, wireless sensor networks, distributed embedded systems and industrial computer engineering. Eduardo Tovar has been consistently participating in top-rated scientific events as member of the Program Committee, as Program Chair or as General Chair. Examples are: IEEE RTSS (Real Time Systems Symposium); IEEE RTAS (Real-Time and Embedded Technology and Applications Symposium); IEEE SDRS (Symposium on Distributed Reliable Systems); IEEE ICDCS (International Conference on Distributed Computing Systems); ACM EMSOFT (Annual ACM Conference on Embedded Software); Euromicro ECRTS (Euromicro Conference on Real-Time Systems); IEEE ETFA (Emerging Technologies on Factory Automation) or IEEE WFCS (Workshop on Factory Communication Systems). He is team leader within the 6th Framework IST Network of Excellence ARTIST2, on distributed embedded systems.

Vahabi, Maryam

PhD Student

Maryam Vahabi received her degree in Electrical Engineering from University of Guilan in 2003. She obtained her Master of Science in Communication Network Engineering from University Putra Malaysia in 2009 and her Master research was on wireless sensor networks. She has joined the IPP-HURRAY! in July, 2009. Currently, she is doing her PhD in CISTER/IPP-HURRAY Research unit. Her current research interests are sensor networks, real-time systems and schedulability analysis.

Vergueira, Marco

Undergrad Student

Marco Vergueira was born in 1988 in Valpaços, Portugal. From an early age acquired a passion for engineering. Currently, he is enrolled in the 3rd year of the ISEP's course in Computer Engineering at the School of Engineering, Polytechnic Institute of Oporto, and is doing is internship at CISTER Research Group, his main research interests are in embedded systems and high level software

Yomsi, Patrick Meumeu

PhD Université Paris Sud, France

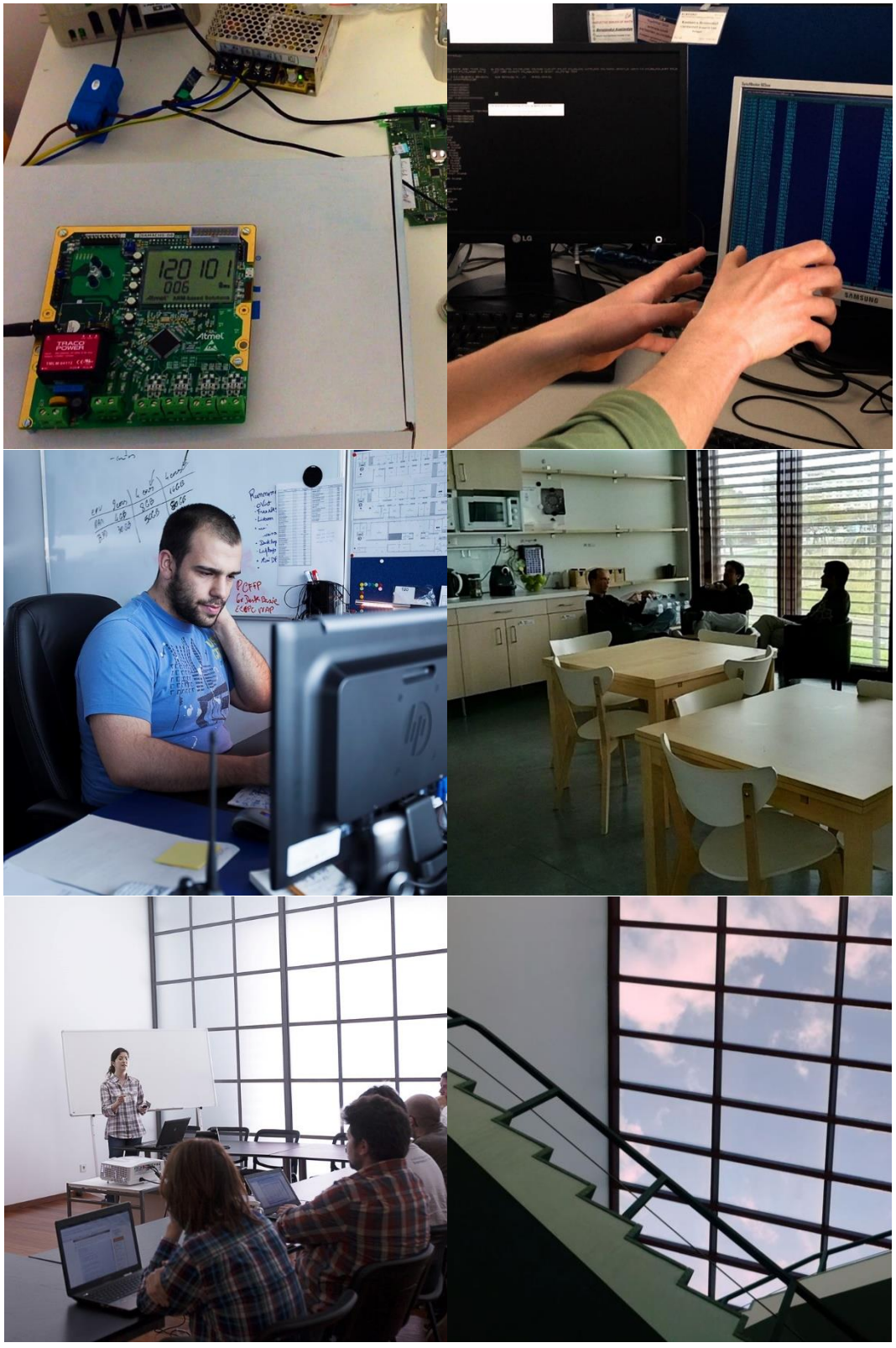
Research Associate

Patrick Meumeu Yomsi received his Ph.D. degree in 2009 from the Université Paris Sud, Orsay in France. After his degree, he worked in a number of research projects addressing various aspects of real-time computing systems. He was successively a member of AOSTE Research Unit at the French National Institute in Computer Science and Control (INRIA) in Paris Rocquencourt, France, then a member of PARTS Research Unit at Université Libre de Bruxelles (ULB) in Brussels, Belgium, and finally a member of TRIO Research Unit at INRIA in Nancy, France. He is currently a Research Scientist at CISTER Research Unit at ISEP/IPP. His research interests include real-time scheduling theory, real-time communication and real-time operating systems.

Facilities

www.cister.isep.ipp.pt/info

CISTER has evolved gradually (in the last 15 years) from a few rooms at ISEP Campus to an entirely new building. This single-home (2000 m2 area) for CISTER is a strong asset which will help the unit to continue to meet the demands and challenges of the current and future projects and to pursue a work plan of high standard that matches the best in the world in the area of real-time and embedded systems.



CISTER
Research Center in
Real-Time & Embedded
Computing Systems

Mailing Address:
CISTER Research Centre
ISEP - Instituto Superior de Engenharia do Porto
Rua Dr. António Bernardino de Almeida 431
4249-015 PORTO
Portugal

Phone: +351-228340502
Fax: +351- 228321159

WWW: http://www.cister.isep.ipp.pt
Email: cister-info@isep.ipp.pt

Building Address:
(please do not use for correspondence)
CISTER Research Centre
Rua Alfredo Allen, 535
4200-135 PORTO
Portugal

GPS: 41.1779,-8.6058