WCRT Analysis for the 3-Phase Task Model in Partitioned Scheduling

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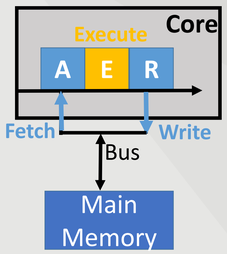
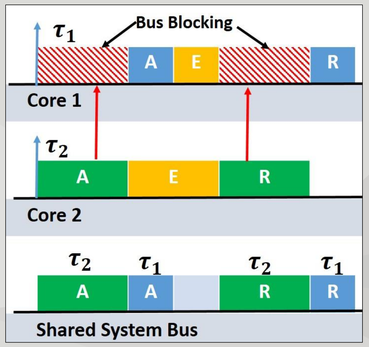
1. Motivation

- **Multicore processors** use a **shared system bus** to **fetch** data/instructions from **main memory**.
- This **sharing** can cause **non-deterministic variations** in the tasks' **execution times** due to **inter-task bus blocking**.
- **Phased** execution models, e.g., **3-phase task model**, are **promising candidates** to circumvent the problem of inter-task bus blocking.
- State-of-the-art bus contention analyses for 3-phase tasks only focus on **global scheduling**.



3-Phase Execution Model



Bus Blocking in 3-Phase Task Model

2. Contributions

- **Bus blocking-aware WCRT analysis** for the 3-phase task model under **partitioned** non-preemptive scheduling.

3. Level-i Busy Window

- Level-i busy window $W_{i,l}$ of core π_l is given by:

$$W_{i,l} = C^{max}_{lp,i,l} + Bus^{max}_{i,l}(W_{i,l}) + \sum_{\tau_h \epsilon hep_{i,l}} (\eta^+_h(W_{i,l}).C_h)$$

Max. blocking from $lp_{i,l}$ | **Max. Bus Blocking** | **Max. interference** from $hep_{i,l}$

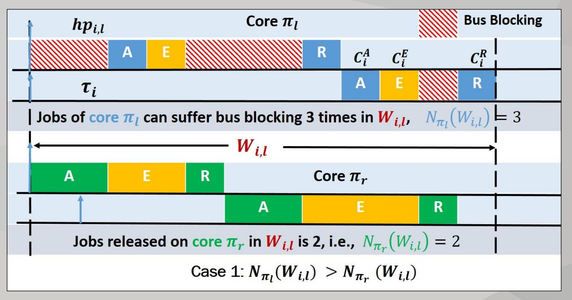
- **Max. number of jobs of** task τ_i that can **execute** in $W_{i,l}$:

$$\eta^+_i(W_{i,l})$$

4. Computing Bus Blocking

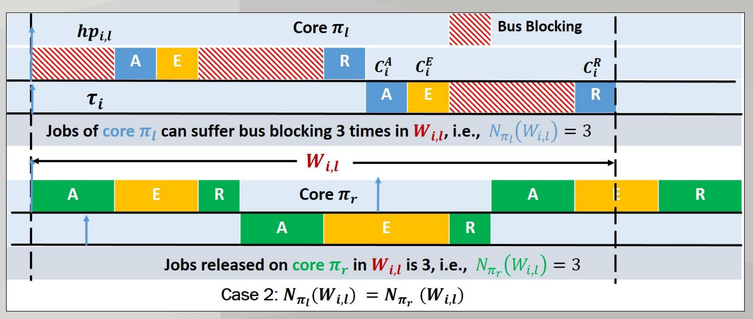
- The maximum bus blocking $Bus^{max}_{i,l}(W_{i,l})$ suffered by the tasks of local core π_l from the tasks of remote core π_r in any **time window** of length $W_{i,l}$ depends on:
- The maximum number of times the **jobs** released on the local core π_l can suffer **bus blocking in** $W_{i,l}$, i.e., $N_{\pi_l}(W_{i,l})$.
- The maximum **number of jobs** released on the remote core π_r that can **cause bus blocking in** $W_{i,l}$, i.e.,$N_{\pi_r}(W_{i,l})$.
- There are three possible cases.

Case 1: $N_{\pi_l}(W_{i,l}) > N_{\pi_r}(W_{i,l})$



- $Bus^{max}_{i,l}(W_{i,l})$ is given by the **sum** of the execution time of **all memory phases** of **all jobs** released on **core** π_r in $W_{i,l}$.

Case 2: $N_{\pi_l}(W_{i,l}) = N_{\pi_r}(W_{i,l})$



- $Bus^{max}_{i,l}(W_{i,l})$ is given by the **sum** of **all memory phases** of **all jobs** (**except** the **smallest A- or R-phase**) of **core** π_r in $W_{i,l}$.

Case 3: $N_{\pi_l}(W_{i,l}) < N_{\pi_r}(W_{i,l})$

- **Extract** N_{π_l} **number** of **A-** and **R-phases** with **higher memory demand** from the **jobs** of **core** π_r released in $W_{i,l}$.
- Sub-case 1: If the **total number of jobs** associated to **extracted memory phases** is **greater** than N_{π_l} then $Bus^{max}_{i,l}(W_{i,l})$ is given by **sum** of **all** the **extracted memory phases**.
- Sub-case 2: If the **total number of jobs** associated to **extracted memory phases** is **equal to** N_{π_l} then one A- or R-phase cannot participate in the bus blocking (similarly to Case 2).
- For sub-case 2, $Bus^{max}_{i,l}(W_{i,l})$ is given by the **sum** of **all** the **extracted memory phases** and then **remove** the **smallest A-** or **R-phase** from the **extracted** memory phases and **add** the **largest A-** or **R-phase** from the **remaining** memory phases of **core** π_r released in $W_{i,l}$.

5. Bus-aware WCRT Analysis

- **Latest start time of R-phase** of k^{th} job of task τ_i of core π_l:

$$s^R_{i,k,l} = C^{max}_{lp,i,l} + \sum_{\tau_h \epsilon hep_{i,l} \setminus \tau_i} (\eta^+_h(s^R_{i,k,l} - (C^A_i + C^E_i)).C_h) + Bus^{max}_{i,l}(s^R_{i,k,l}) + (k-1).C_i + (C^A_i + C^E_i)$$

C_h: **WCET** of τ_h | $Bus^{max}_{i,l}(s^R_{i,k,l})$: **Bus Blocking** until **start time** of the **R-phase** of τ_i | $(k-1).C_i$: **Previous jobs** of τ_i | $(C^A_i + C^E_i)$: **WCET** of **A-** and **E-phase** of τ_i

- **Response time** of k^{th} job of task τ_i of core π_l:

$$R_{i,k,l} = s^R_{i,k,l} + C^R_i$$

C^R_i: **WCET** of **R-phase** of τ_i

- WCRT of task τ_i of core π_l:

$$R^{max}_{i,l} = \max_{k \epsilon [1, \eta^+_i(W_{i,l})]} \{R_{i,k,l}\}$$

6. Future Work

- **Experimental evaluation** and **comparison** with the **state of the art.**

References

[1] Claudio Maia, Geoffrey Nelissen, Luis Nogueira, Luis Miguel Pinho, and Daniel Gracia Perez. Schedulability analysis for global fixed-priority scheduling of the 3-phase task model. In RTCSA, pages 1–10, Hsinchu, Taiwan, August 2017. IEEE.

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