Towards the Certification of Multicore Platforms in the Avionics Domain

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Motivation and challenges

- Demand for extra functionality
- Performance per watt ratio increase
- Multicore paradigm shift
- Resource sharing
- Non- deterministic behavior
- Safety critical applications
- CAST-32 position paper
- Software- based solutions

Sources of non-determinism

Caches

- Shared caches
- Effect on WCET
- Preemptions overhead
- Partitioned caches
- Local overhead accounting
- Cache usage profile
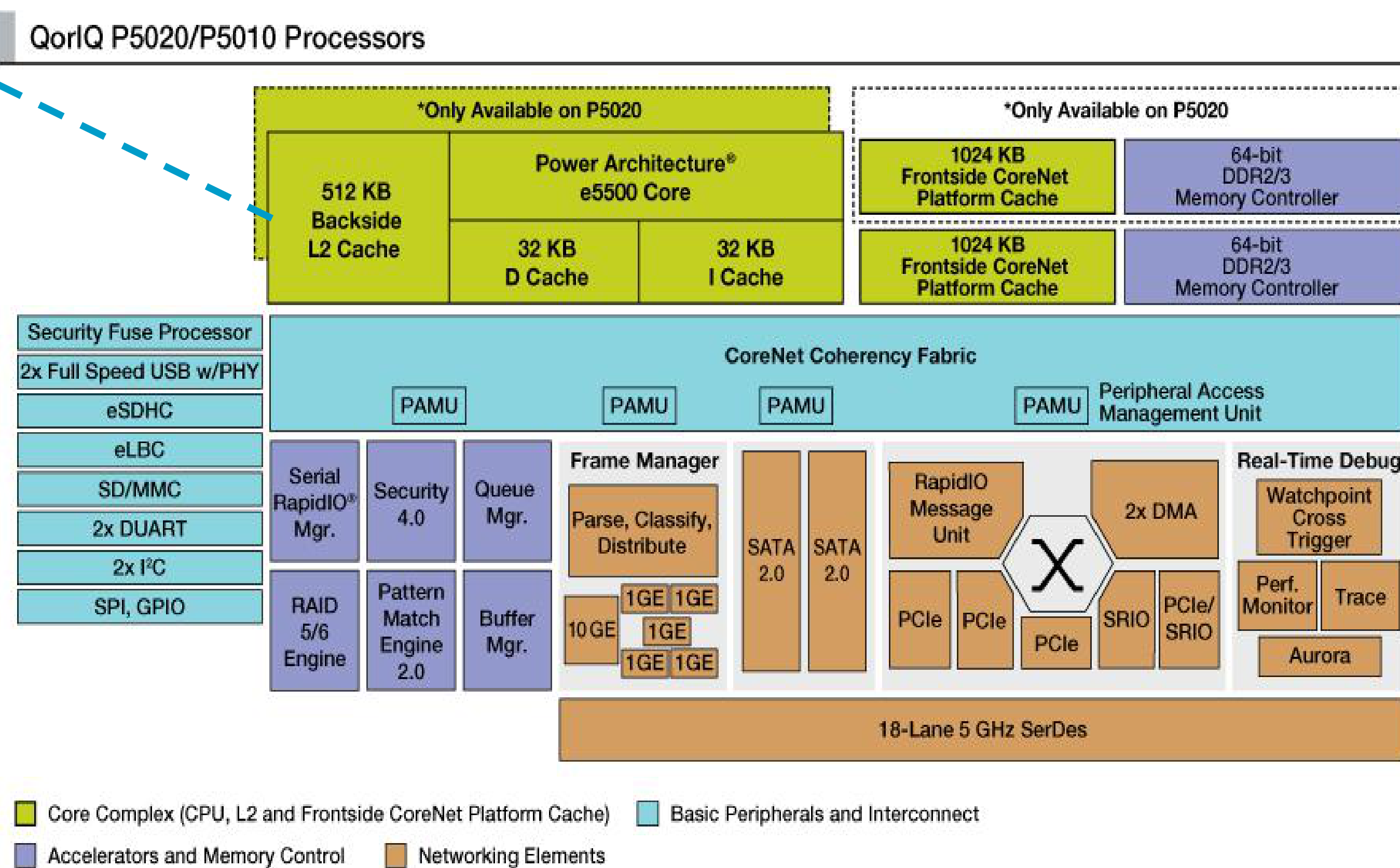
Memory

- Shared memory
- Race conditions
- Data starvation
- Deadlocks
- Live-locks

I/O Subsystem

- Interact with environment
- Shared I/O devices
- Direct Memory Access (DMA)
- Traffic between cores and memory
- Cache coherency
- DMA interference

QorIQ P5020/P5010 Processors

*Only Available on P5020

512 KB Backside L2 Cache | Power Architecture® e5500 Core
32 KB D Cache | 32 KB I Cache

*Only Available on P5020
1024 KB Frontside CoreNet Platform Cache | 64-bit DDR2/3 Memory Controller
1024 KB Frontside CoreNet Platform Cache | 64-bit DDR2/3 Memory Controller

Security Fuse Processor
2x Full Speed USB w/PHY
eSDHC
eLBC
SD/MMC
2x DUART
2x I²C
SPI, GPIO

CoreNet Coherency Fabric

PAMU | PAMU | PAMU | PAMU | Peripheral Access Management Unit

Serial RapidIO® Mgr. | Security 4.0 | Queue Mgr.
RAID 5/6 Engine | Pattern Match Engine 2.0 | Buffer Mgr.

Frame Manager
Parse, Classify, Distribute
10GE | 1GE 1GE | 1GE | 1GE 1GE

SATA 2.0 | SATA 2.0

RapidIO Message Unit
PCIe | PCIe | PCIe
2x DMA
SRIO | PCIe/SRIO

Real-Time Debug
Watchpoint Cross Trigger
Perf. Monitor | Trace
Aurora

18-Lane 5 GHz SerDes

Core Complex (CPU, L2 and Frontside CoreNet Platform Cache) | Basic Peripherals and Interconnect
Accelerators and Memory Control | Networking Elements

Conclusions

- There is a strong industrial drive towards developing hardware-based solutions
- We firmly believe on the merits of software- based mechanisms
- Partitioned caches is the way forward for safety critical applications
- Cache related preemption delay should be handled locally on each core
- Better bounds can be achieved by differentiating between buffered and non-buffered traffic
- Using scratchpad for allocating I/O data can reduce the interference and coherency issues

References

- "Certification authorities software team (cast), position paper (cast- 32) multicore processors," Certification authorities in North and South America, Europe, and Asia, May 2014.